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ESD – A Potentially Dominant Failure Mechanism

DfR Solutions – Electronic Polymers Webinar

Date: July 16, 2015

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What is ESD?

- Electrostatic Discharge, or ESD, is a single-event, rapid transfer of electrostatic charge between two objects, usually resulting when two objects at different potentials come into direct contact with each other. ESD can also occur when a high electrostatic field develops between two objects in close proximity. ESD is one of the major causes of device failures in the semiconductor industry.

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ESD Models

- There are three (3) predominant ESD models for IC's:
  - 1) the *Human Body Model (HBM)*;
  - 2) the *Charged Device Model (CDM)*; and
  - 3) the *Machine Model (MM)*.

ESD Models

- The HBM simulates the ESD event when a person charged either to a positive or negative potential touches an IC that is at another potential.
- The CDM simulates the ESD event wherein a device charges to a certain potential, and then gets into contact with a conductive surface at a different potential.
- The MM simulates the ESD event that occurs when a part of an equipment or tool comes into contact with a device at a different potential. HBM and CDM are considered to be more 'real world' models than the MM.

Design for ESD Prevention: What Do You Need to Do?

- ESD Protection is necessary at the IC, component package and system level
  - Different approaches are needed to achieve reliable protection
- Designing for ESD impacts both the product design and the manufacturing process controls
- What technologies are available to assure a reliable ESD protected product?
  - At the IC level
  - At the component package level
  - At the system level

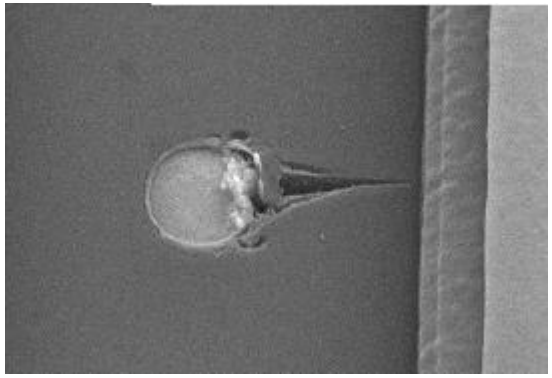
Component Failure Mechanisms: ESD

- Objects moving with respect to each other transfer charge
  - Amount depends on materials, speed, proximity
  - Dissipation depends on conduction paths
- Extremely large voltages possible
  - Dry environment
  - Materials with easily stripped electrons
  - No discharge path
- Human perception > 5 kV
  - Circuits long since destroyed

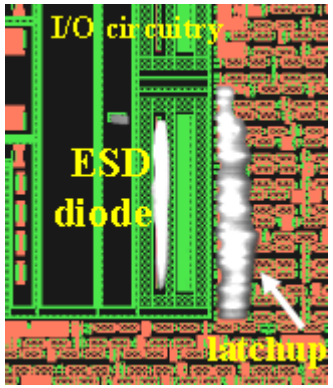
Component Failure Mechanisms: ESD

- Two primary failure mechanisms:
  - Electric field-induced
    - Silicon dioxide breakdown ~ 7e8 V/m
      - 60Å oxide destroyed at ~ 4.2V
      - Shorts gate permanently
    - Fields could push carriers into insulators
      - May just degrade performance
  - Thermal destruction
    - Any resistance in path subject to local intense heating
      - Contacts, vias, and junctions
      - Weakest link goes first
    - May also produce "walking wounded"
      - Increased leakage
      - Increased resistance
      - Softened junctions
- All protection techniques fail eventually
  - Class A,B, & C specifications are 1kV, 2kV, & 4kV, respectively

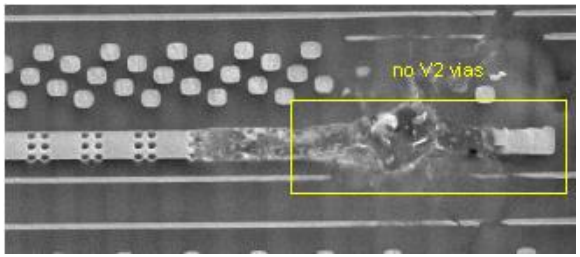
Component Failure Mechanisms: ESD Examples



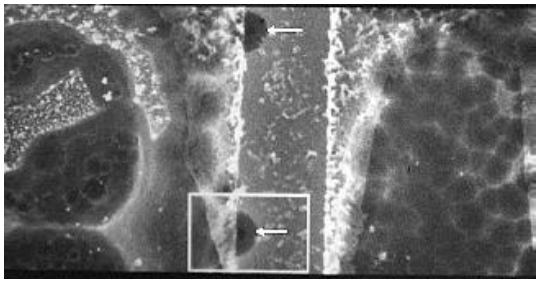
SEM of P/N junction
Source: Frank, EDFAS, 2004

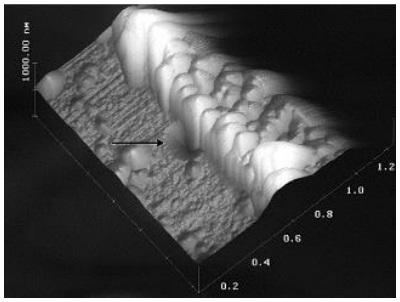


Light emission of latchup in logic circuitry
Source: Frank, EDFAS, 2004

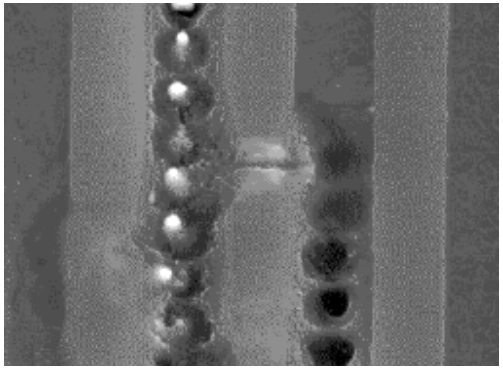


SEM of metal line damage
Source: Putnam *et al*., EDFAS, 2004

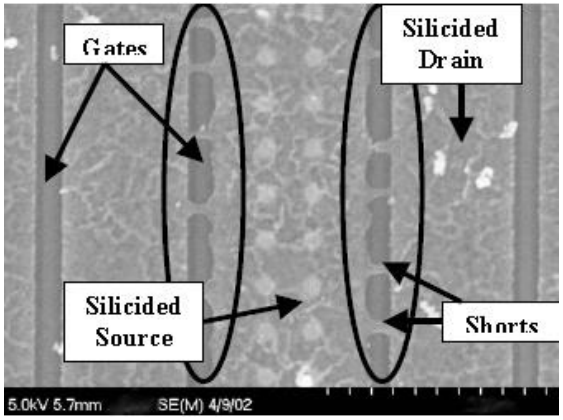




SEM & AFM of lateral ESD on line
Source: Colvin *et al*., EDFAS, 2004



SEM: HBM test on NFET
Source: Putnam *et al*., EDFAS, 2004



SEM of silicide shorts in SOI device
Source: Prejean *et al*., EDFAS, 2004

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Design Practices for ESD

- Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  - Identify all ESD Sensitive Parts on drawings
  - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
- Consider the entire System (Design) as ESD Sensitive

ESD Design Practices (cont.)

- Use ESD Protection on all susceptible parts (not just System I/Os)
  - Box or System I/O
    - ESD Rating < Class 2 IEC (4000V) MANDATORY
  - Internal Components (not exposed to outside connectors)
    - ESD Rating <= Class 1 ANSI (0-999V) MANDATORY
    - ESD Rating < Class 2 ANSI (2000V) WHEREVER POSSIBLE
- High Speed, RF and GaAs parts will be particularly sensitive to ESD
  - GaAs Parts are typically rated as Class 0 (<250V) or Class 1A (<500V) – ONLY THE BEST PROTECTION DESIGN AND HANDLING PROCEDURES WILL PREVENT DAMAGE TO THESE PARTS!
- Place ESD sensitive components and traces to avoid locations where the board may be handled
- Consider ESD as well as RF shielding
- Where possible install protective devices before ESD sensitive parts
- Avoid Coupled ESD events – Do not route traces to ESD sensitive parts near lines connected to the outside world

ESD Design Practices (cont.)

- Perform Circuit analysis to insure effectiveness of ESD protection (Class 2 ANSI [2000V] for internal, IEC level 2 [4000V] for I/O)
- Test Boards and Systems for Internal and I/O ESD tolerance
- ESD Protection devices must be connected to a good ground to accommodate up to 30A ESD spikes.
  - If upset of operating circuits is to be avoided, a separate Earth ground should be used

ESD Sensitive Parts (Pin Sensitivity)

- Any pin of a discrete ESD sensitive part (FET, Transistor, etc) may need protection (if not connected to a supply)
- Input pins
  - Can be sensitive since they have little or no built-in ESD protection
  - Especially on high speed devices like GaAs ICs or discretes,
- Pins other than inputs (on an ESD sensitive part)
  - Can also be sensitive because an ESD pulse can affect internal voltage levels
  - Any improperly terminated or unprotected pin can be a conduit for ESD
- Supply pins
  - Provide reference bias connections
  - Should not need additional protection (as long as they are connected to the power supply)
- Outputs of logical or functional parts designed with active (usually buffered) output stages
  - May have clamping diode protection to the supplies and may not need additional protection – check the part ESD rating

Evaluate Potential ESD

- If ESD sensitive parts are used in design, the circuitry connected to device pins should be evaluated
  - Insure that it provides "attenuation" to prevent voltage in excess of the parts ESD rating from developing in case the pin or connected traces are contacted during board handling or system assembly.
- Often the recommended circuit components for operation of the part will provide adequate ESD protection.
  - This should be verified by analysis or simulation and extra protection added as required to limit the voltage seen at the part.
  - Assumptions for analysis/simulation
    - 2000V,1.5K, 100pf for Internal circuits
    - 4000V, 330 Ohms, 150pf for I/Os

Design for ESD Prevention: ESD IC Device Specifications

- What should you be concerned about?
  - Completely different specification methods for ESD protection of components are commonly used
  - Designers may need to gather comparable data points from differing graphs and tables.
  - Some differentiators to look for and investigate further are outlined below

- IEC Rating: Verify that the ESD protection device is guaranteed to meet or exceed specifications in IEC 61000-4-2.

- Contact versus Air Discharge: Verify that identical specifications are being compared. Some devices are documented with high air discharge ratings, which can be incorrectly compared with the normally lower contact discharge ratings. Contact ratings are fairly repeatable, whereas air ratings vary.

IEC 1000-4-2 COMPLIANCE LEVEL	MAX TEST VOLTAGE, CONTACT DISCHARGE (kV)	MAX TEST VOLTAGE, AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

- Clamp Voltage: Choose a device with a maximum clamp voltage at a given peak current well below the level that the protected devices can tolerate. The lower, the better.

- Pulse Current: Beware of misleading approximations of peak power capacity. It can usually be improved by specifying a shorter peak duration.

ESD IC Device Specifications

- Response Time: Faster-acting devices reduce the width of the pulse transferred, and these devices can help attenuate the peak clamp voltage.
- Parasitic Capacitance: Added capacitance degrades I/O signal rise and fall times. On lower-speed signals, this stray capacitance can be lumped into or can displace the need for EMI capacitors.
- Parasitic Inductance: Higher impedance in the clamp path (to VDD or ground) can increase the effective system clamp voltage.
- Multistrike Capability: Verify that the protection designed-in can survive the expected life of the system. Resultant field failures are difficult to diagnose and can manifest themselves in unexpected functional errors, or even data loss.
- Integration and Matching: High-speed differential signals, such as in IEEE 1394, benefit from matched loading on the positive and negative lines of each pair. ESD protection products with multiple devices per package (such as thin-film silicon) can have intrachip device-to-device parasitic impedance matching of less than 0.1%. Unitary packages, however, may vary as much as 30% interchip matching. Printed-circuit-board (PCB) signal routing restrictions may also indicate a need for tight multidevice integration.

Design for ESD Prevention & IC Design Rule Checking

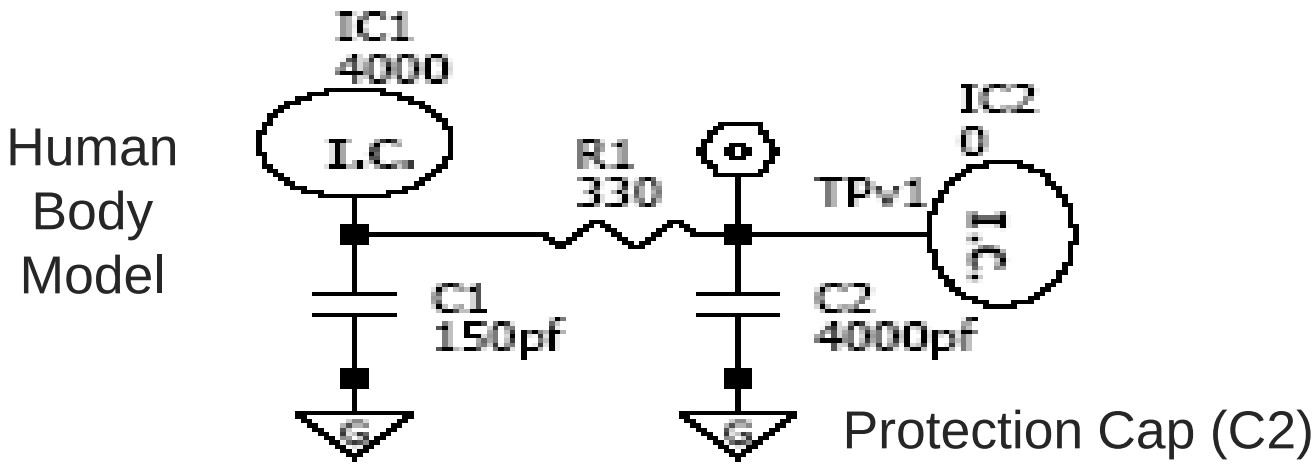
- Many ESD design rules
- Two common types of design rule verification/compliance
  - Design Rule Checking (DRC): standard DRC tools with ESD marking layers
    - Example: Mentor Graphics Calibre PERC
      - Rule 1: Primary Protection for I/O Pad
        - For each net in design, IF net is connected to IO Pad THEN check for up HBM diode and down HBM diode IF diode(s) missing THEN ESD Error
      - Rule 2: Secondary Protection for I/O Pad
        - For each net in design, IF net is connected to input buffer and IO Pad THEN check for CDM up diode and CDM down diode check if CDM resistor exists and is correct value IF diode(s) missing or resistor incorrect THEN ESD Error
  - Net-oriented: in-house tools for circuit analysis.

ESD Protective Device Options

- Passive Networks
  - Capacitors – Simple, Low cost
  - Band-pass filters – Somewhat more complex, good ESD protection
- For lower speed devices
  - Schottky Diodes – Simple, but capacitance loads HF circuits
  - Diode Clamping Arrays – Good for LF circuits and outputs
- For higher speed devices (requiring low capacitance)
  - Low capacity protection diodes (<1 pf) – Robust, Good HF compromise
  - Polymer ESD (PESD) Protection devices (<0.25 pf)
    - Excellent HF characteristics, small size 0402, 0603
    - PESDs have limited Pulse life, good parts withstand 100 to 1000 strikes
    - Operating voltage typically 5V, available to 12V, Trigger Voltage 100, 150V

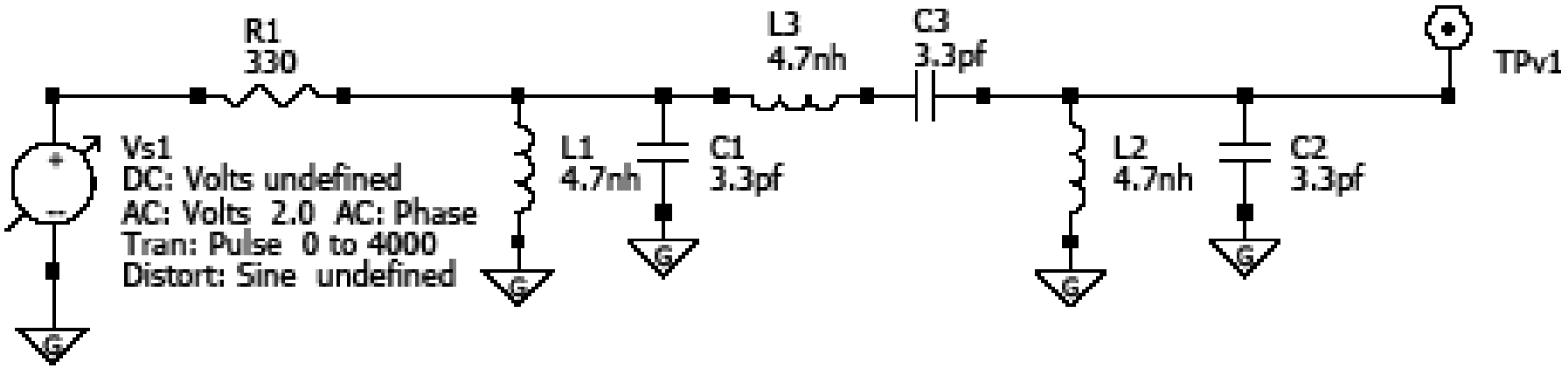
Simple Capacitive Protection

- Use to provide ESD protection on bypassed pins for ESD sensitive devices, or at Supply input connections
  - Make sure capacitance (C2) is significantly larger than the Human Body Model (>> 150pf) to minimize developed voltage (approx 28 times or 4000pf for protection of a Device with an ESD sensitivity of 150V)
  - May add a Resistor to bleed off charge (from C2)
  - Use 200V rated Cap (for C2)



Filters

- Band-pass filters can be used for higher frequency applications and can be effective for RF system inputs
- Very Robust circuit with good protection



Band-pass Filter 850-2GHz, 50 Ohm Impedance
C1,C2,C3 rated at 100V

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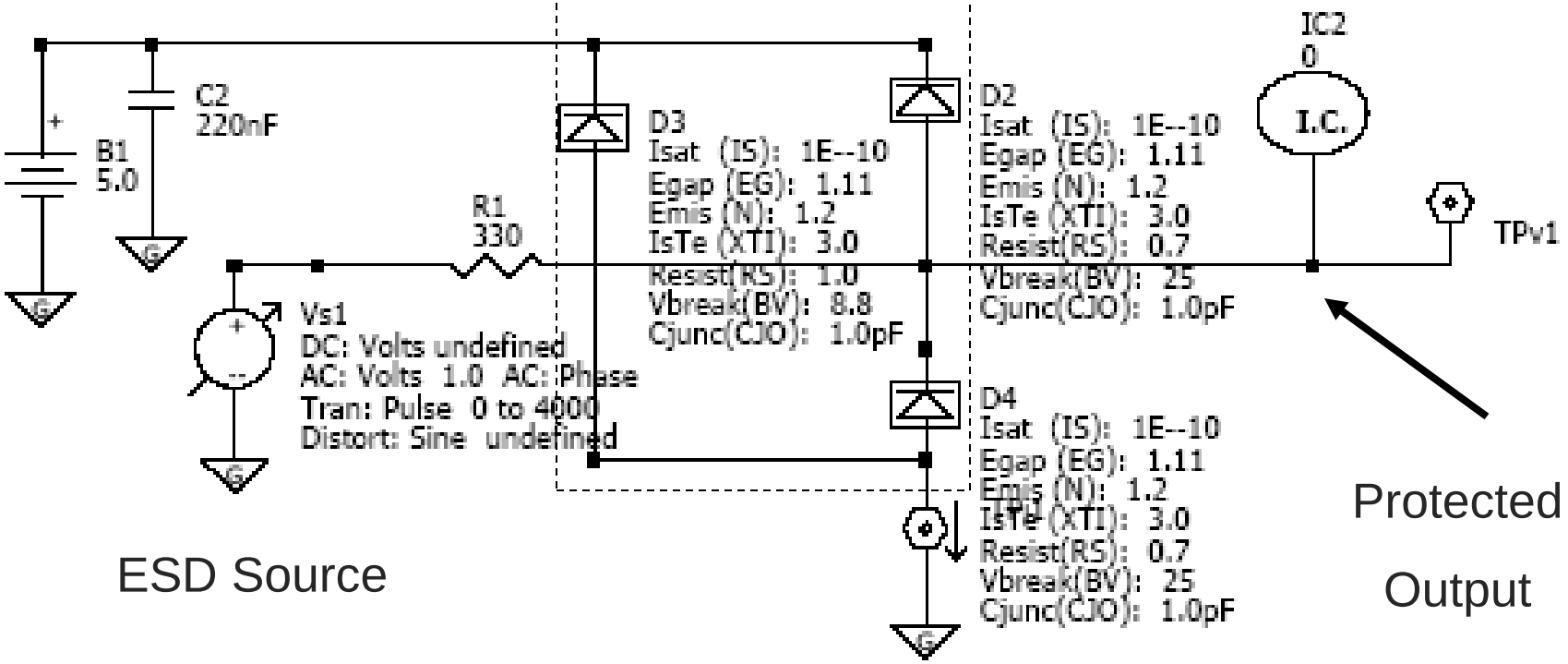
Protection with Clamping Diodes

Protection Diode
Array (CM1213-01)



ESD Source

Protected Output

ESD at output is clamped at approximately 14V with 4000V ESD hit through 330 Ohm resistance

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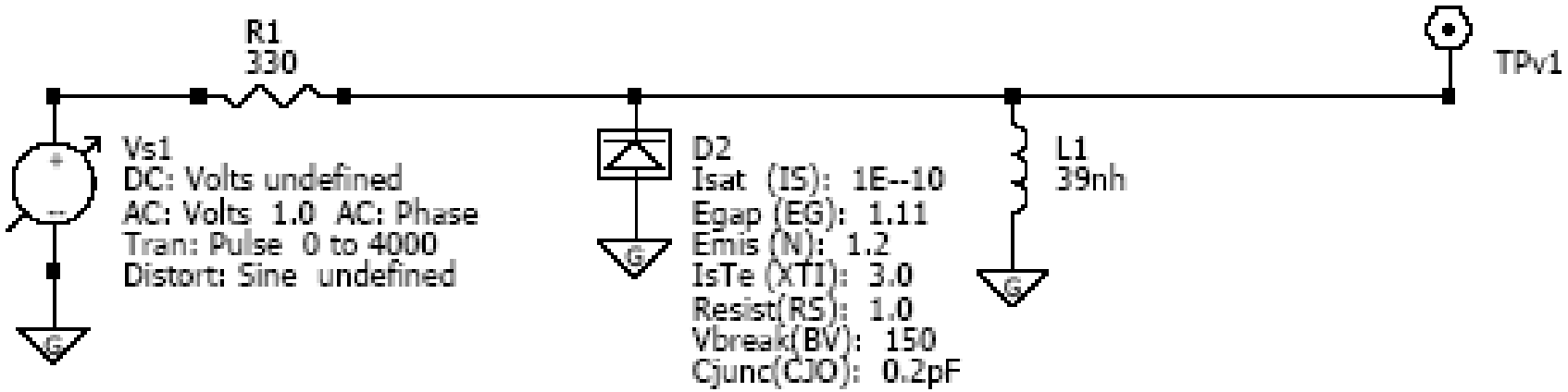
PESD (Polymer ESD) plus Inductor

IEC HBM

PESD, Trigger
Voltage =150V



- The Inductor shunts lower frequency energy to ground, removing stress from the PESD.
- Provides better protection than the PESD alone and extends life of the PESD
- The PESD can be used alone for wider bandwidth operation

Summary of ESD Design Guidelines

- Design ESD Protection for External (System) I/Os to IEC HBM Class 2 (4000V, 150pf, 330 Ohm) Including:
  - RF or signal inputs
  - Control and System I/Os that DO NOT have built in protection to the required limit
- Design ESD Protection for Internal ESD sensitive parts to meet ANSI 20.20 Class 2 (2000V)
- Know the ESD rating of every part used
- Select parts (where possible) to meet ANSI 20.20 ESD level Class 2 or better (2000V)
- Parts rated less than Class 2 should have additional protection circuitry added to protect the board during handling

ESD Design Guidelines (cont.)

- For External (System) Inputs use Robust protection:
  - Band pass filter
  - PESD plus Inductor (for Severe condition use PESD + Filter)
- For Internal ESD Sensitive pins use:
  - Single bypass Cap (where possible)
  - Filter if needed
  - PESD or PESD plus Inductor
- Any Pin of an ESD sensitive part may be at Risk If It is NOT:
  - Connected to a supply plane
  - Adequately decoupled to GND (~4000pf @200V)
  - Protected by a "filter" network (simulate for an ESD hit)
- External (System) Output or I/O
  - Use low capacitance Clamping diodes (1pf)
  - PESD if required for speed (.25pf)

Failure Analysis Techniques

- Returned parts failure analysis always starts with Non-Destructive Evaluation (NDE)
- Designed to obtain maximum information with minimal risk of damaging or destroying physical evidence
- *Emphasize the use of simple tools first*
- (Generally) non-destructive techniques:
  - Visual Inspection
  - Electrical Characterization
  - Time Domain Reflectometry
  - Acoustic Microscopy
  - X-ray Microscopy
  - Thermal Imaging (Infra-red camera)
  - SQUID Microscopy

Failure Analysis Techniques

- Destructive evaluation techniques
  - Decapsulation
  - Plasma etching
  - Cross-sectioning
  - Thermal imaging (liquid crystal; SQUID and IR also good after decap)
  - SEM/EDX – Scanning Electron Microscope / Energy dispersive X-ray Spectroscopy
  - Surface/depth profiling techniques: SIMS-Secondary Ion Mass Spectroscopy, Auger
  - OBIC/EBIC
  - FIB - Focused Ion Beam

Examples of Lab Testing

- Electrostatic discharge test – Human body model
- Test method was MIL-STD-883, method 3015.8

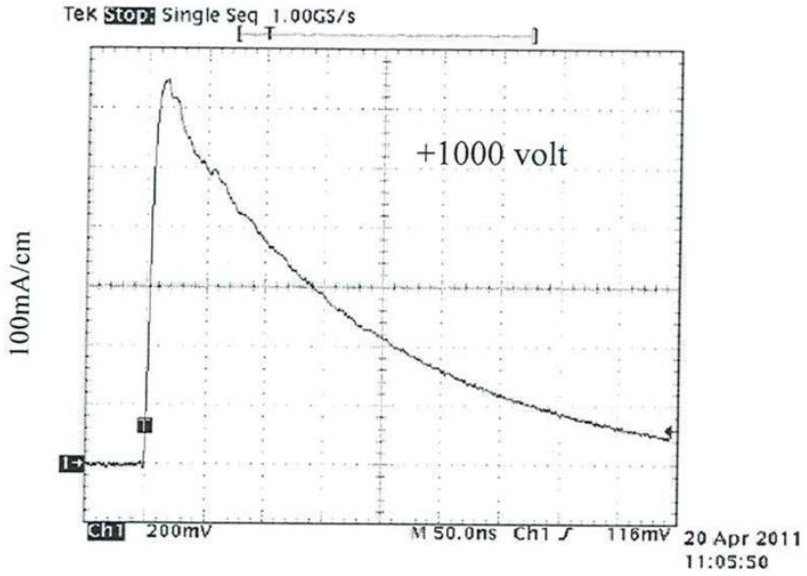


Figure 1. Prestress test positive pulse waveform.

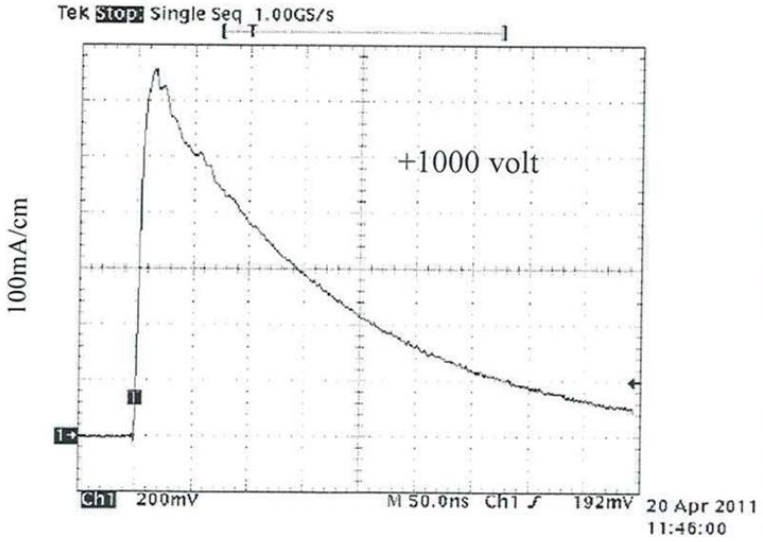


Figure 2. Post stress test positive pulse waveform.

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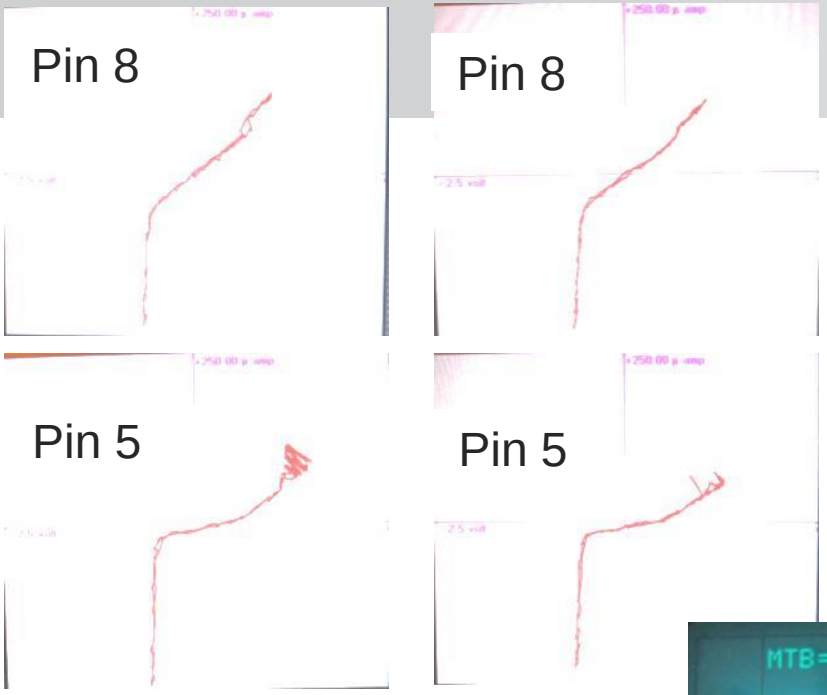
Results
Electrical

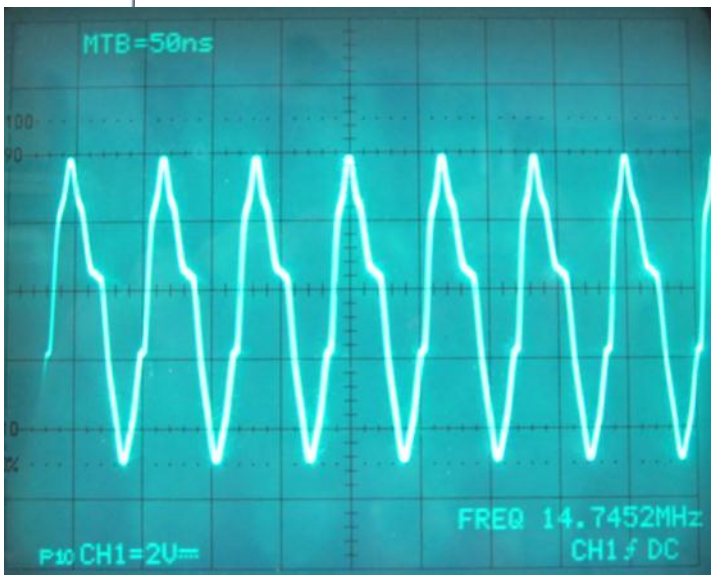
Curve tracing example.

ESD damage was suspected in Part B



Curve tracing was done between power (pin 8), output (pin 5) and ground (pin 4). There is a slight difference in traces for the output signal between Part A and Part B.

Part B was powered at 3.3V and output monitored with a 10K ohm load. It operated at the specified frequency (14.745M Hz) but the wave form was not a square wave as expected.



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Trying to distinguish between EOS & ESD

- Often difficult to distinguish between EOS/EOL (electrical overstress and electrical overload) and ESD. Some rules of thumb:
- ESD damage
  - Small failure sites
  - Not always visible without deprocessing
  - No visible evidence at the package level
- EOS damage
  - Large areas of damage
  - Burned silicon and metallization
  - Sometime visibly evident package damage

Trying to distinguish between EOS & ESD

- EOS: Thermal overstress to a component's circuitry
  - Short Pulse Width Failure – Junction Spiking
  - Long Pulse Width Failures – Melted metallization and open bond wires
  - Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. By that time an Al spike is said to have shorted the junction, damaging the device permanently.

Images of ESD Damage

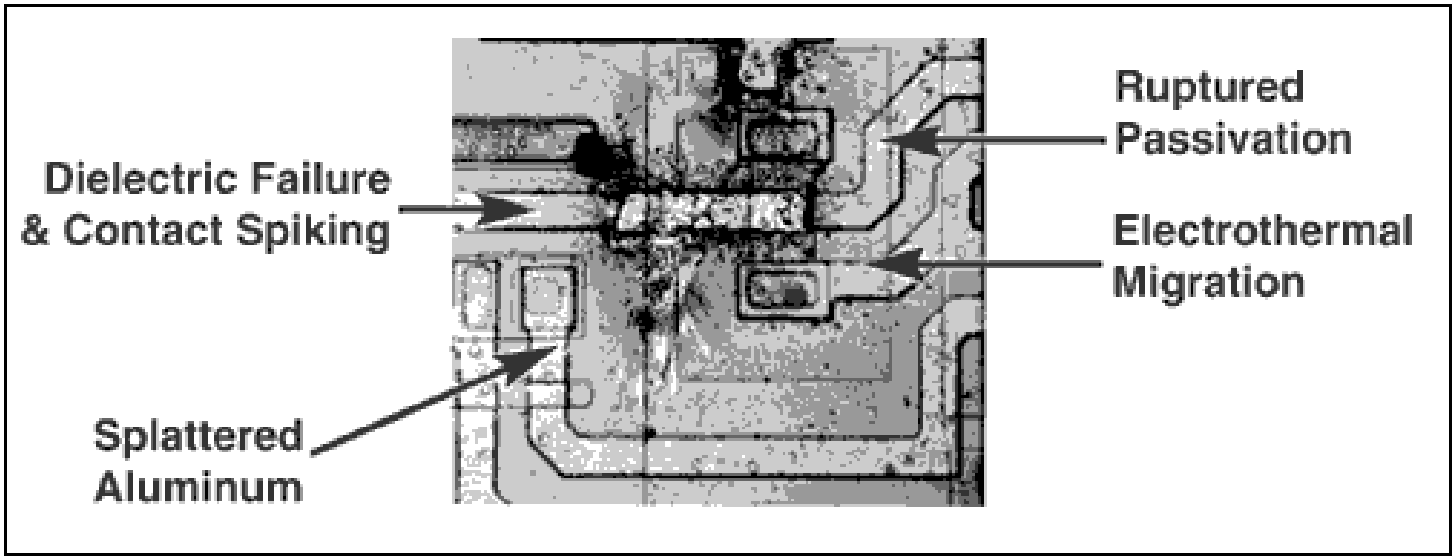


Figure 1. ICs with inadequate ESD protection are subject to catastrophic failure—including ruptured passivation, electrothermal migration, splattered aluminum, contact spiking, and dielectric failure. (Image courtesy of Maxim IC)

ESD Failures: Latent Failures

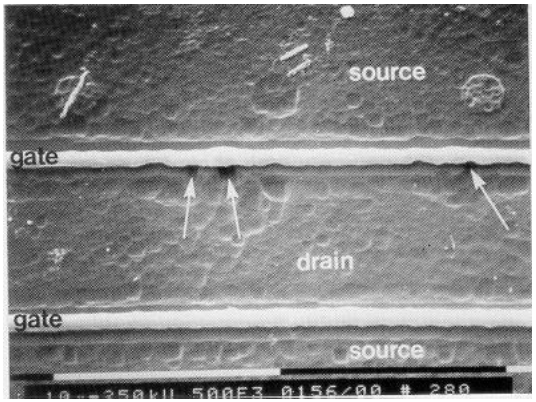
Latent Failures

- ESD events not only impact assembly yields, but also can produce device damage that escapes testing and causes latent failures in the field.
- Devices with latent ESD defects have been referred to as "walking wounded" because they are degraded but still function
- Latent damage can occur when an ESD event is not sufficiently strong to destroy a device
  - Device continues to function and is still within data-sheet limits
  - Device can be subjected to numerous weak ESD events, with each new event further degrading a device until total failure
  - No known practical way to screen for walking wounded devices
  - Damage to insulators: weakening of the insulator structures, leading to accelerated breakdown and/or increased leakage
  - Damage to junctions: lowering the lifetime of minority carriers with consequent bipolar transistor gain loss; increasing resistance in forward biased state; increasing leakage in reverse biased state
  - Damage to metallization: weakening of the conductor, leading to increased resistance or increased rate of electromigration

ESD Failure Modes

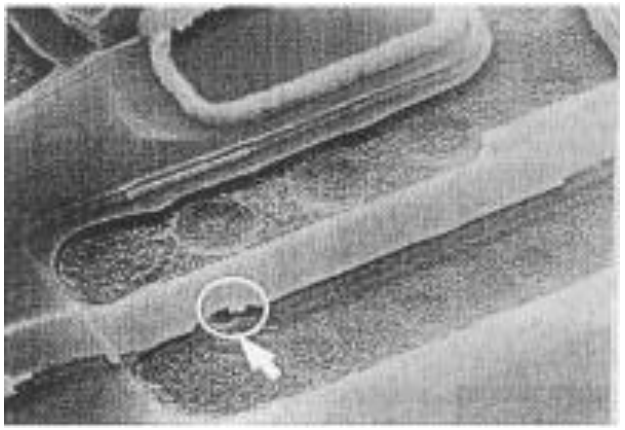
ESD Failure Modes

- Different ESD models tend to produce different types of failure and require different types of control and protection.
- Basic failure mechanisms include
  - Oxide punchthrough
  - Junction burnout
  - Metallization burnout



Drain-junction damage in an NMOS after HBM stress. Note the thermal damage to silicon. Image courtesy of TI.

Gate-oxide damage to an input buffer after CDM stress. Note the rupture in gate oxide. Image courtesy of TI



Thanks

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