Let it flow

Craig Hillman

While much of the fame and glory, and money, may go to semiconductor manufacturing, the fabrication of printed circuit boards (PCBs) can often be a more difficult and challenging endeavor. Complex composites with anisotropic properties that change with time and temperature can be difficult to predict and control. An excellent example of this was a root-cause analysis performed on a board-mounted power supply that experienced a thermal event.

One of the challenges in performing a failure analysis on a PCB that experienced a thermal event (i.e., burned) is that typically any evidence of root cause has effectively gone up in smoke. When faced with this type of challenge, it is best to take a three pronged approach. The first step is to examine the same area on PCBs from similar date codes. This helps identify possible design flaws that may have contributed to the event. The second step is to investigate the PCB around the vicinity of the thermal event. This helps to identify any evidence of possible manufacturing defects. The third step is investigating the actual burn site itself. Information gained from the first two activities often helps greatly increase the value of this final step.

Observations of cross-sections from the first step (similar area, different PCB) showed indications that resin was unable to flow during lamination. Inability to flow resulted in some areas starved of resin. Other areas may have experienced severe stresses, resulting in crack propagation. The differentiation is based upon the edges of the anomaly. In the resin starvation image, the edge of the anomaly is rounded. In the cracking image, the edge of the anomaly is pointed (*Figure 1*)

The resin starvation seemed to be affiliated with the edges of the copper foil, where it would be the most difficult for the resin to flow (*Figure 2*).

It was noted that the crack opening affiliated with the plated through holes (PTHs) was larger than the crack opening affiliated with the cracks within the prepreg and the laminate. This likely was due to when the cracks initiated. Cracks within printed circuit boards (PCBs) can occur during processes of elevated stress, either thermal or mechanical. For most PCB processes, these high stresses occur during

- Lamination
- Drilling
- Reflow

Cracks with small openings suggest exposure to one elevated stress event. Cracks with larger openings suggest exposure to two or more elevated stress events. The annular opening around the PTHs would be an area that would be susceptible to resin starvation. Areas of resin starvation create sites for crack propagation during drilling operations. Pre-existing cracks would then tend to increase in size

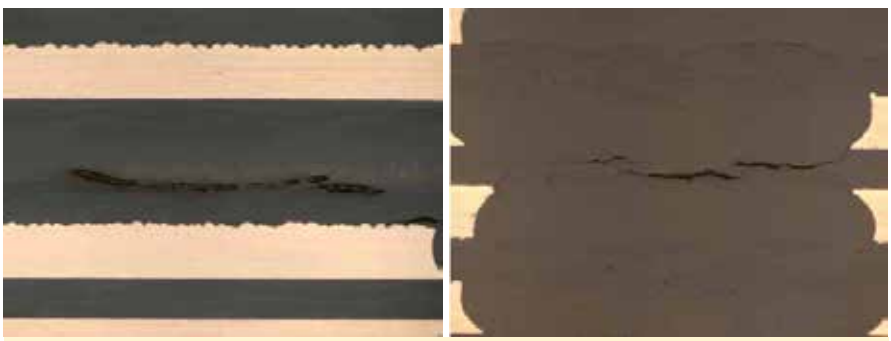

Figure 1. Resin starvation (left) and cracking (right).

Figure 2. Illustration of resin starvation.

Figure 3. Void/delamination from resin starvation is linked to cracks eminating from the copper foil.

after exposure to reflow conditions. Cracks with smaller openings most likely initiated during or after reflow.

While cracking or resin starvation can cause issues in PCBs, such as the occurrence of conductive anodic filament (CAF) formation, separately they are not necessarily an indication of root-cause. However, the second step of the investigation provided more definitive evidence. Surprisingly, more than one driver for failure was identified.

The first potential driver for failure was the intersection of the two types of anomalies. As seen in *Figure 3*, the void/delamination from resin starvation linked to cracks emanating from the copper foil. This junction provided a clear and complete path for metal migration from the internal plane to the plated through via. When the step of path formation is eliminated, CAF or metal migration can occur relatively rapidly (minutes to hours), even under relatively benign conditions, due to capillary condensation. The condensation event can immediately create an electrolytic cell and can extract contaminants from the epoxy resin.

Continued inspection of the cross-section then noted a second potential failure inducing flaw. The anomaly was internal deformation, specifically of the copper foil and the prepreg material. The deformation of the copper foil resulted in spacings as small as 20 microns between internal planes. Is this degree of separation sufficient to have induced infant mortality due to dielectric breakdown?

Dielectric failure of laminate material will be dependent upon the direction of the electrical arc. Dielectric strength and dielectric breakdown are the values of electrical field stress that result in dielectric failure. Dielectric strength is measured perpendicular to the lamination direction and is very high (approximately 30kV/mm). Dielectric breakdown is measured parallel to the lamination direction. Because the fiber/epoxy interface provides a convenient path for electrical discharge, the electrical field stress necessary for intralayer breakdown is typically much lower (approximately 3 kV/mm).

At first pass, a review of these numbers would seem to suggest that TDDB was unlikely. Assuming a 15 micron spacing and a potential of 48 VDC, the resulting electric field stress of 3200 V/mm is an order of magnitude below the specified dielectric strength. However, there are two potential scenarios were the expected 30 kV/mm strength may not be present.

Figure 4. Another potential failure-inducing flaw: deformation of the copper foil resulted in spacings as small as 20 microns between internal planes.

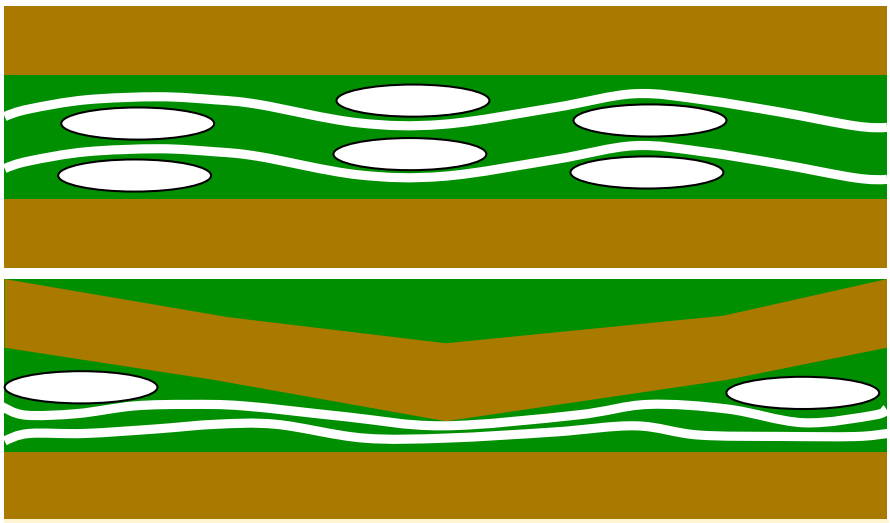

Figure 5. During deformation of the internal planes, the laminate weave can become displaced.

As seen in *Figure 5*, during deformation of the internal planes, the laminate weave can become displaced. If the displacement is severe, then there is a possibility that the fibers of the two plies will come into contact. This contact provides a path between the plies. It was also observed, and confirmed by Tyco, that nesting occurs within this stackup. Nesting, which is when glass fibers come into contact with the copper foils, provides the path from the copper to the plies. The combination of these two physical artifacts can create a path for TDDB that is similar to intralayer breakdown as opposed to interlayer breakdown. In this situation, the lower value of dielectric breakdown, approximately 3 kV/mm, may be more appropriate.

In addition, dielectric strength and breakdown measurements are performed at room temperature. The operating conditions of this device are known to be at elevated temperatures. It is general knowledge that the dielectric strength and breakdown drops as a function of temperature, but there is little quantifiable data that would allow a prediction of how the dielectric strength or breakdown may have degraded for this particular layout and material set. Two examples are known by DfR. One reference measured a 20% reduction in dielectric strength between room temperature and 100˚C. The second reference measured up to an order of magnitude reduction in time to failure between the temperatures of 60˚C and 80˚C.

So, which is the smoking gun? The cracking or the deformation? The conclusive answer was based on the final stage of the activity, inspection of the actual burn site. With information from the first two steps guiding the activity, it was noted that there were no plated through vias in the area of severest damage. Instead, it seemed to originate between two internal planes.

While identifying the root cause was relatively straightforward, preventing it from occurring in the future is much more challenging. Larger amounts of resin can prevent resin starvation and can allow the PCB vendor to reduce the amount of pressure being applied during lamination. However, larger amounts of resin, in combination with the thick copper planes, can greatly reduce time to failure during power cycling. How to optimize so no one failure mode dominates (or, preferably, even occurs)? Physics of failure.