Accurate Quantitative Physics-of-Failure Approach to Integrated Circuit Reliability

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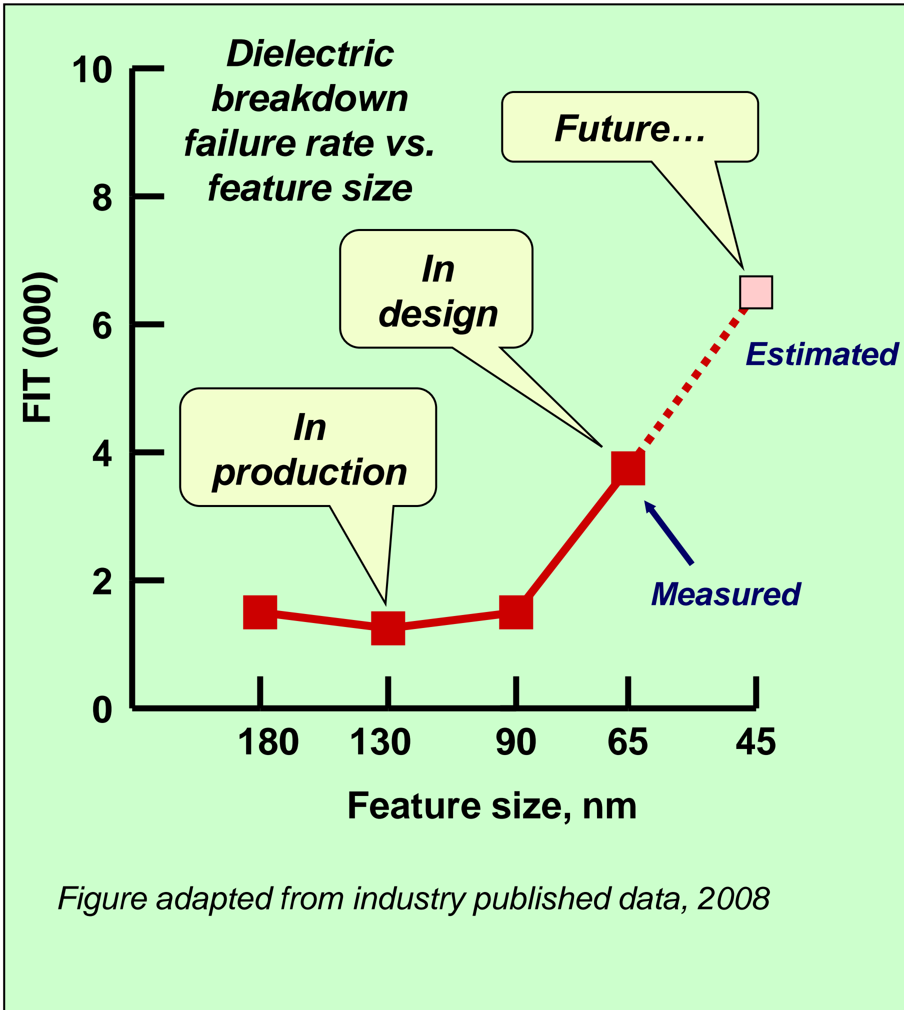
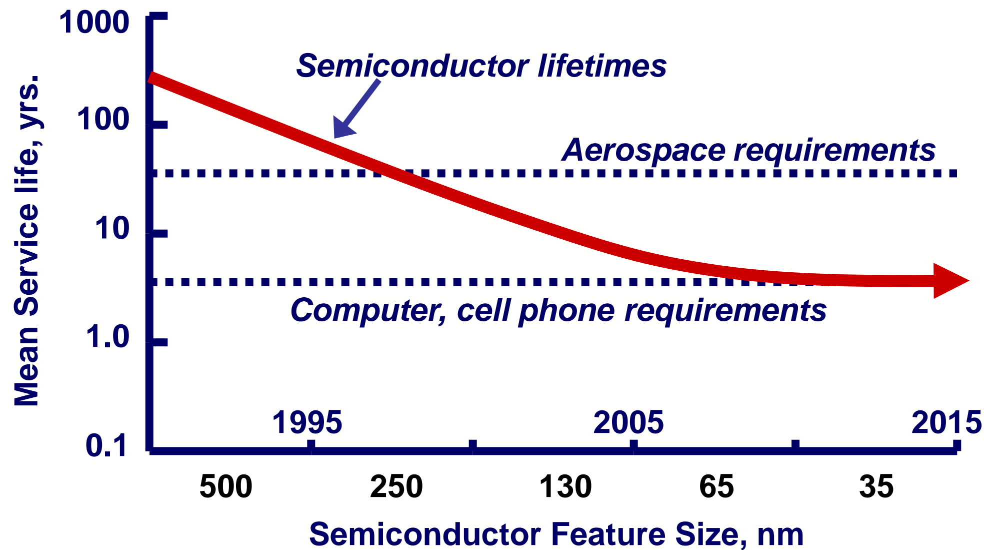
Trading Reliability for Performance



Failure rate data/projection from the aerospace industry (same application environment at each node)

- Introduction of new technology corresponds to projections of Moore's Law
  - 70% feature scaling every 2-3 years
  - *Smaller and Faster circuits cause*
    - *Higher current densities*
    - *Lower voltage tolerances*
    - *Higher electric fields*
  - *Inherent Si-based failure mechanisms are manifested at these minute feature sizes*

High Reliability Requirements



- High Performance Commercial Off The Shelf (COTS)
  - *Consumer purchasing drives the marketplace*
    - *Performance (Moore's Law trending) versus Reliability*
    - *Newest, smallest, fastest technology is designed for 3-5 year lifetime*
  - *Growing need to predict lifetime of these components for aerospace, defense and other high performance (ADHP) industries*
    - *Anticipated lifetime of 10 to 30 years for these electronics*

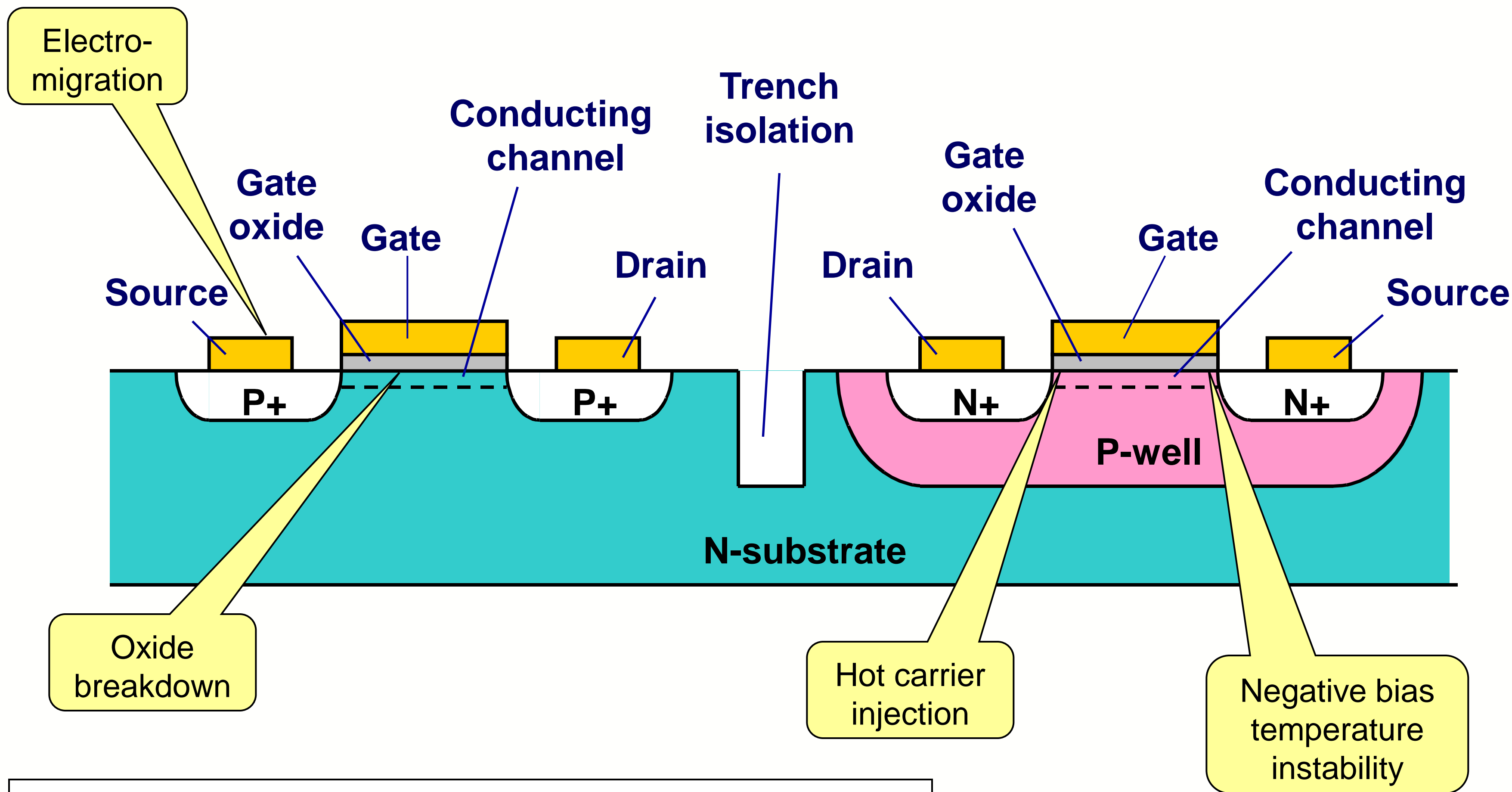
Modeling a Solution

- Create an easy to use software tool that can be used by multiple disciplines of engineers
  - Accessible component data (datasheet limitations)
  - Anticipated field conditions and component stresses
  - With minimal access to manufacturer data
    - Sometimes only censored data is available
- Back to the fundamentals
  - Transistor theory and circuit analysis
  - Physics-of-Failure (PoF) degradation models

"The notion that a transistor ages is a new concept for circuit designers," … aging has traditionally been the bailiwick of engineers who guarantee the transistor will operate for 10 years or so…But as transistors are scaled down further and operated with thinner voltage margins, it's becoming harder to make those guarantees… transistor aging is emerging as a circuit designer's problem.

IEEE Spectrum, June 2009

Issues Inherent to CMOS Design



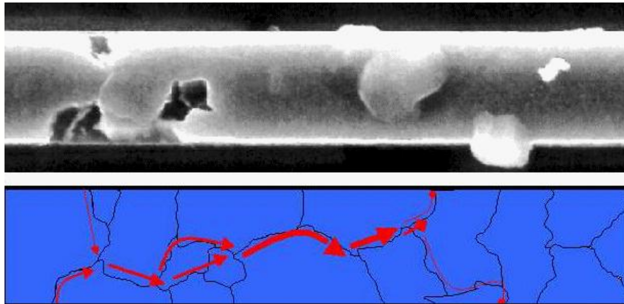
Artist depiction of CMOS transistors

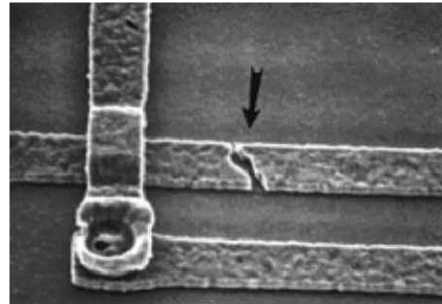
Mitigation Through Design? TDDB

- Time Dependent Dielectric Breakdown (TDDB)
  - *Not so time dependent after all*
    - During feature scaling, the gate oxide thickness is scaled down
    - Power supply voltage is approximately the same as previous node
    - Increase in electric field on gate dielectric due to smaller thickness
    - What does this mean?
      - Instead of cumulative degradation from multiple breakdown sites causing failure after an undefined interval, one (1) breakdown site may cause immediate failure
  - *Mitigated by:*
    - Doping the dielectric (however, each dopant causes other issues)
    - High-k and Low-k dielectrics (scaling issue remains)
    - Changing the geometry/topography of transistor features (expensive)

Mitigation Through Design? EM

- Electromigration (EM)
  - *Dependent on conductor materials*
    - Effects have already been mitigated a few times, but not solved
      - Black's equation predicts time-to-failure
      - Latest conductor change to a better Al + Cu alloy (~0.13 micron)
  - *Mitigated by:*
    - *Changes in trace geometries, polygons versus 90° angles, and trace width*
    - *Drastic change in materials, i.e. carbon nanotubes or graphene*
    - *Additions of more copper, silver, gold, etc.*

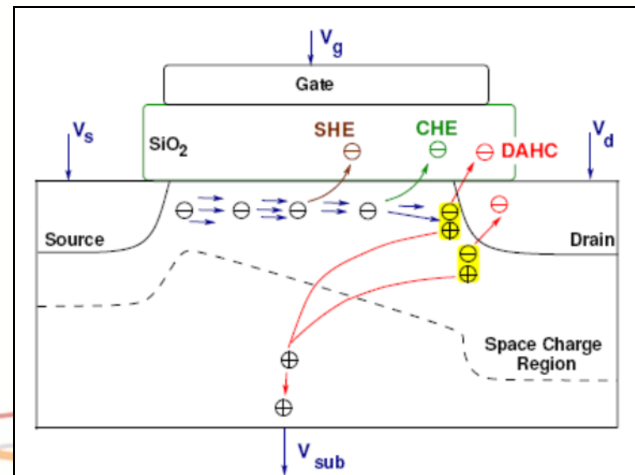




Damaging effects of EM on conductors

Intrinsic Behavior and Wearout

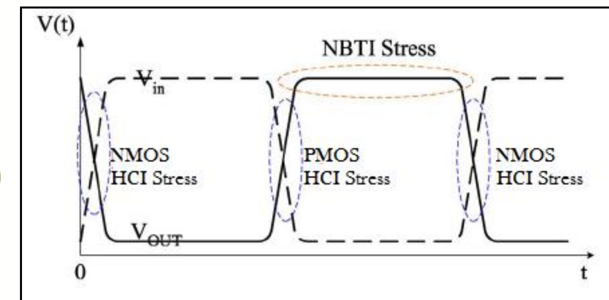
- Wearout *because of* transistor design
  - MOSFETs operate using electric fields ("field effect")
  - BTI and HCI are driven by electric fields
  - New architectures experience these modes, i.e. FLASH memories
    - Floating gate transistor makes use of forced HCI and Fowler-Nordheim tunneling to store charge on the floating gate
  - Phenomenon of electrons and holes (carriers) gaining sufficient energy to overcome the direction of induced current and become injected in the gate oxide



Depiction of hot carrier effects on MOSFET

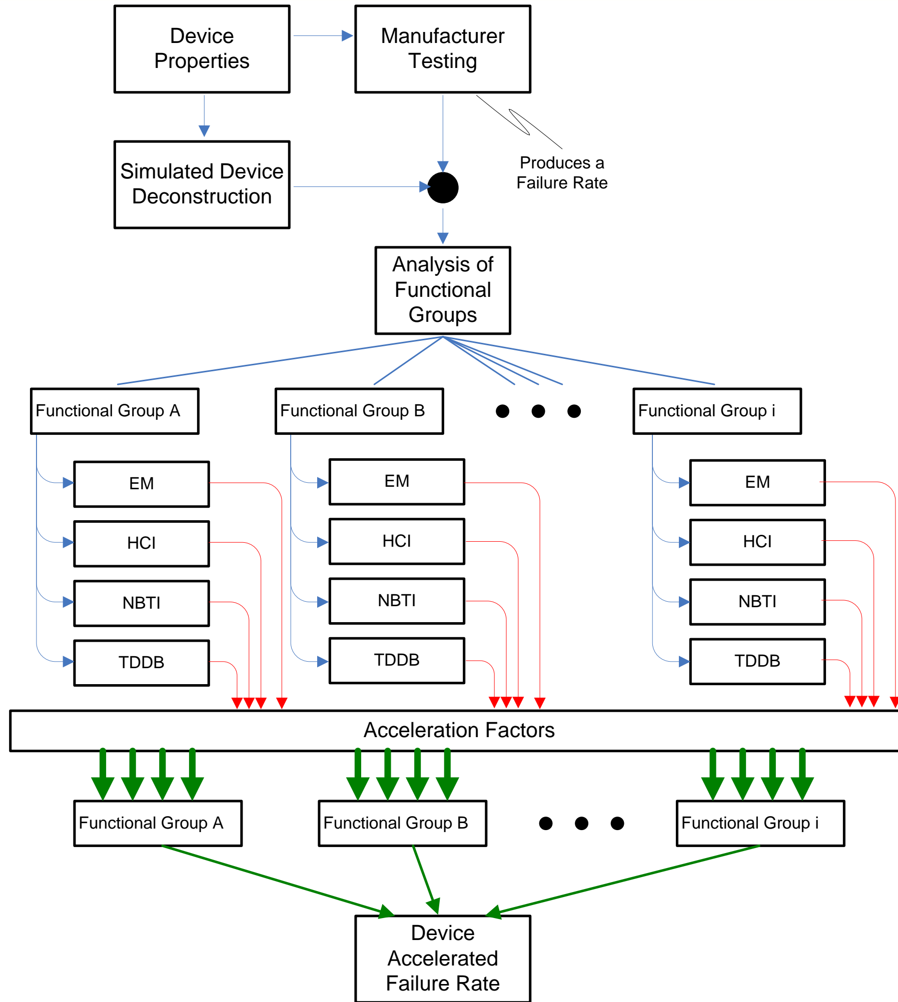
Intrinsic Behavior: HCI and BTI

- Hot Carrier Effects or Injection (HCI) Characteristics
  - Caused by a single carrier gains sufficient kinetic energy, or
  - Multiple carriers undergoing collisions that force them out of the directional path of electric field (the conducting channel)
  - HCI has inverse Arrhenius relationship
    - Activation energy -0.2 to -0.1 eV
    - Lower temperatures (~35 to ~55° C) increase vulnerability
- Bias Temperature Instability
  - Combined bias & temperature stresses are required for activation
    - Fluctuations in temperature (overall device + self heating property)
    - High temperatures cause molecular instability
    - Requires lower electric fields than HCI
  - Trap formation from electric fields are worse under negative bias (positive bias is ~90%+ recoverable)



Transistor stress states relating to HCI/NBTI damage (V_{in}/V_{out} curve)

IC Lifetime Prediction Methodology



- Models the simultaneous degradation behaviors of multiple failure mechanisms on integrated circuit devices
- Devised from published research literature, technological publications, and accepted degradation models from:
  - NASA\JPL
  - University of Maryland
  - Semiconductor Reliability Community

Generic, Industry Accepted Models

- Parameters that drive failure
  - Temperature
  - Current and Current Density
  - Voltages
- Extrapolate from test to field

EM $$\lambda_{EM} = A_{EM} J^n \exp(\frac{-E_{aEM}}{\kappa T})$$

HCI $$\lambda_{HCI} = A_{HCI} (\frac{I_{sub}}{W})^m \exp(\frac{-E_{aHCI}}{\kappa T})$$

TDDB $$\lambda_{TDDB} = A_{TDDB} A^{\frac{1}{\beta}} V_{gs}^{a+bT} \exp(\frac{c}{T} + \frac{d}{T^2})$$

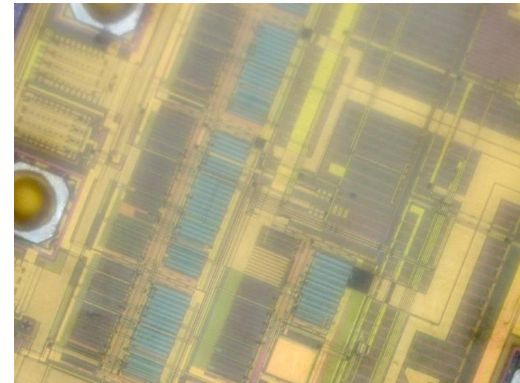
NBTI $$\lambda_{NBTI} = A_{NBTI} V_{gs}^{\frac{1}{\tau}} [\frac{1}{1 + 2\exp(-\frac{E_1}{\kappa T})} + \frac{1}{1 + 2\exp(-\frac{E_2}{\kappa T})}]^{\frac{1}{\tau}}$$

A_{EM}, A_{HCI}, A_{TDDB}, A_{NBTI}, E_{aEM}, E_{aHCI}, n, m,α, β,τ,a, b, c, d, E_1 and E_2 are all technology-related parameters.

APEX EXPO IPC

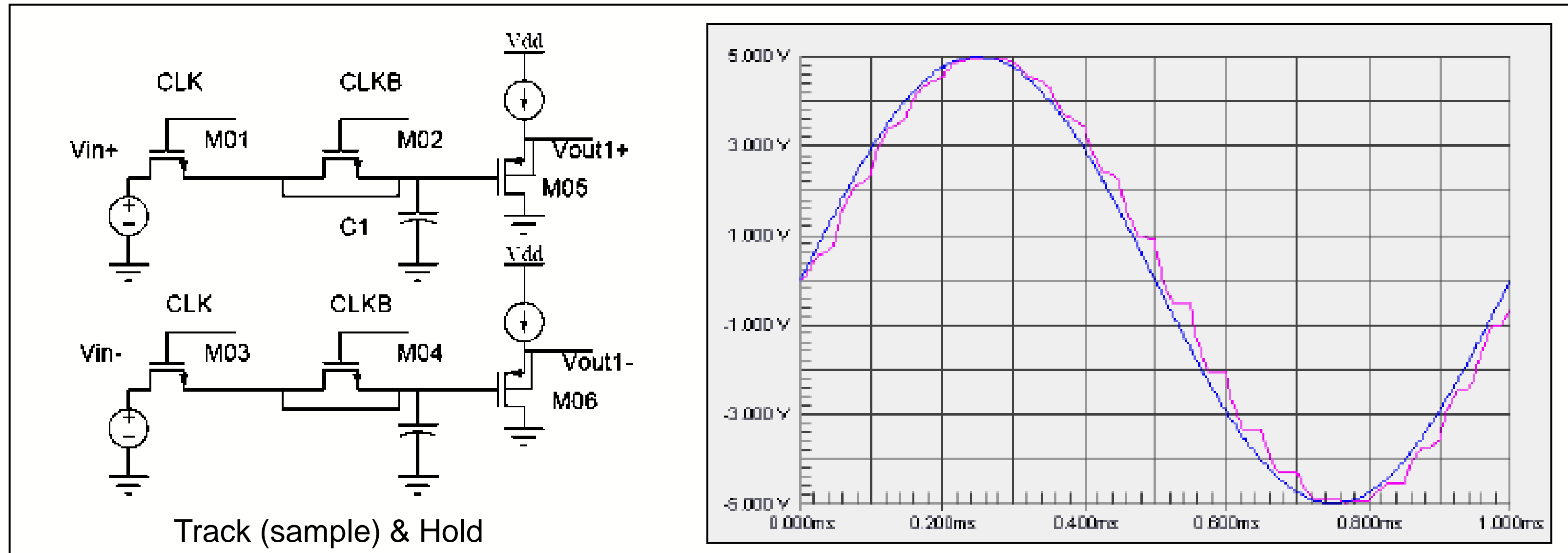
What Influences Failure Rate?

- Integrated circuit materials and complexity
  - Information gathered from component documentation
    - Technology node or feature size (i.e. 90nm)
      - Corresponding material set (e.g. Si, GaAs, SiGe, GaN and SOI)
    - Functional complexity
      - Identified as functional groups within a circuit
    - Operating conditions
      - Voltages, frequencies, currents, and temperature
- Degradation mechanisms
  - PoF knowledge and analysis
    - Transistor stress states
    - Functional group susceptibility
    - Electrical and thermal conditions



Transistor Stress States

- Establish relevancy of failure mechanisms and inputs into PoF algorithms based on
  - Quantity and location of transistors within circuit
  - Probabilistic likelihood of applied operation conditions through background simulation of each functional group



Transistor stress state analysis on Track and Hold functional group

Mathematical Theory

- Model of a device failure rate considering the tiers of system and device level inputs
  - λ_T is the failure rate of the device under analysis
  - λ_i is the normalized failure rate of a failure mechanism within a given functional group
  - $K_{i,F}$ is a constant defined by the weight percentage of functional group F as it affected by the ith failure mechanism
  - P_F is the probability of functional group failure from one functional group cell
  - N_F is the total number of cells in each functional group
  - N is the total number of functional groups across all types
- Acceleration factors can be applied at the transistor level to extrapolate from known device test conditions to a known system field environment

$$\lambda_T = N \times \sum (N_F / N) \times P_F \times \sum (K_{i,F} \times \lambda_i)$$

Snapshot of the Software Tool

IC Reliability Prediction Tool v1.3

Part | Model | Test | Help

Enter the identification information for the IC to be analyzed:

Part Manufacturer	National Semi
Part Number	ADC124S021
Part Description	453-00001
Production Years	Over 5 Years

Select the technology node of the IC to be analyzed:

Node Size	350 nm

Enter the quantity of each function group (e.g., sample
each functional group can typically be found in a parts
in a description of the component features.

Sample & Hold	16384
PreAmp	16384
1st Stage Comparator	8192
2nd Stage Comparator	4096
SRAM (bits)	0
DRAM (bits)	0
Ring Oscillator (stages)	0

IC Reliability Prediction Tool v1.3

Part | Model | Test | Help

Enter the results from integrated circuit testing.

Number of Failures	0
Number of Devices	25
Test Duration (hrs)	1000
Device Duty Cycle (%)	31.25
Confidence Level	50%

Enter one or more operating modes for the IC being tested. Each operating mode can be specified with either a Fixed Temperature or a pre-defined Temperature Profile. The analysis results will be averaged across all temperatures and operating modes specified. The 'Duration' values are used as weights when computing the average across operating modes.

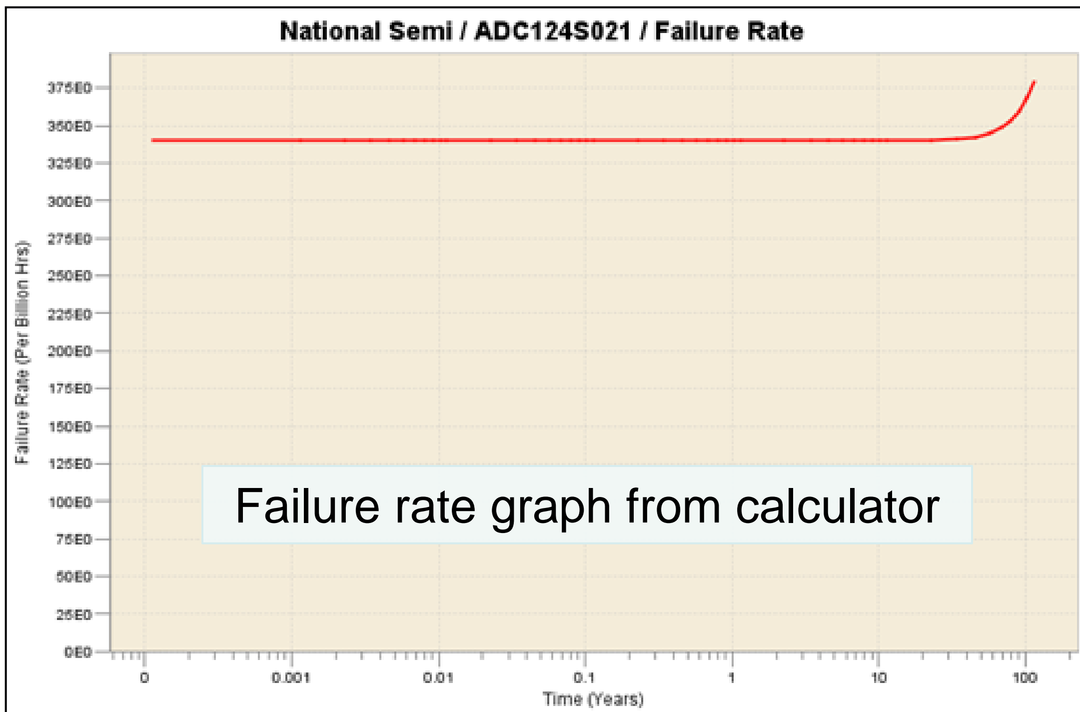
	Temp Profile	Temp (C)	Freq (MHz)	Core (V)	Supply (V)	Duration
1	Arizona		500	1.2	3.3	1.0
2						
3						
4						

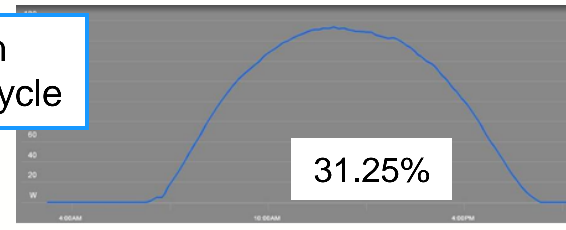
Enter the test parameters used for all operating modes:

Temperature (C)	85
Frequency (MHz)	500
Core Voltage (V)	1.2
Supply Voltage (V)	3.6
Nominal Core Voltage (V)	1.2

- **Inputs:**
  - Component information
    - Feature size
    - Complexity
    - Test data
    - Operating modes
    - Electrical conditions
  - System Information
    - Temperature profiles
    - Duty cycle
  - Confidence level
- **Outputs:**
  - Device reliability
  - Device failure rate

Example: National Semi 12-bit ADC



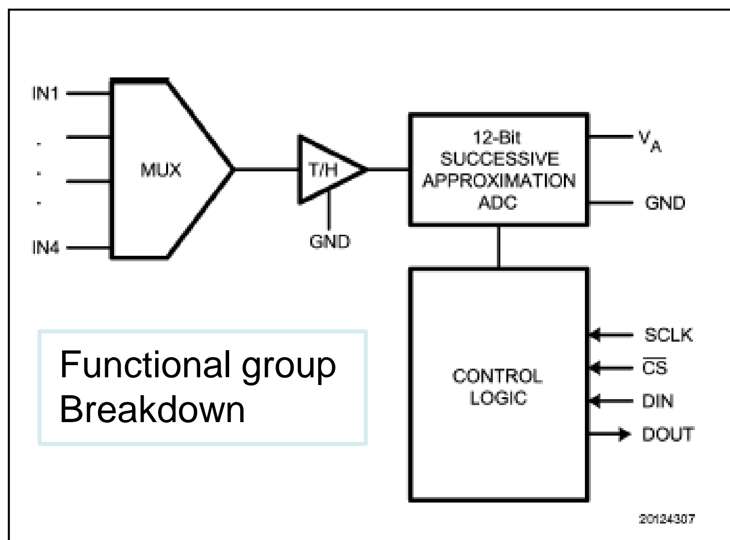


Peak Temperature (°C)	Percentage of Calendar Year
40	4.1%
	17.8%
	21.9%
	12.6%
60	20.8%
70	22.7%

System Temperature Profile

Part Number	Process Technology	Field Voltage (V)	Test Voltage (V)	Field Temperature (° C)	Test Temperature (° C)
ADC124S021	350nm	3.3	3.6	Profile	85.0

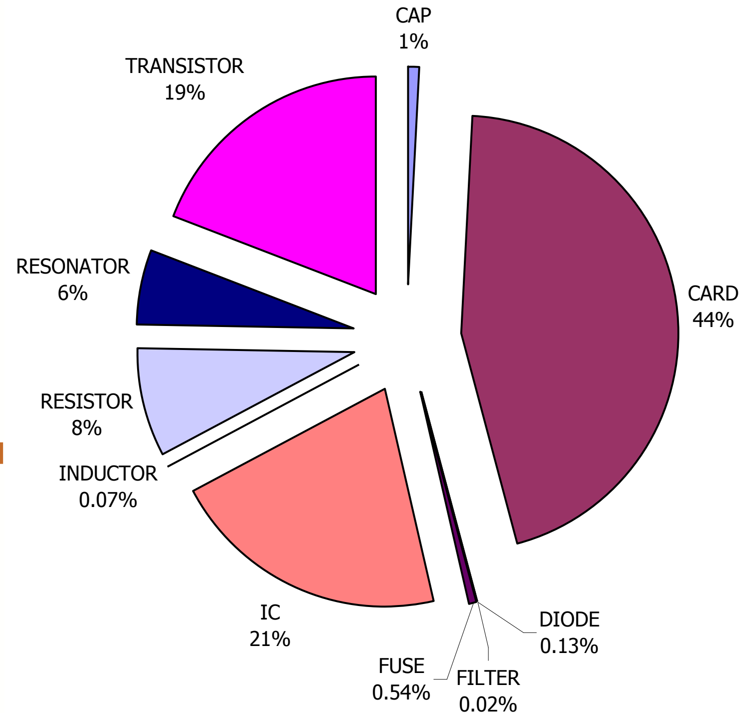
Device characterization



The resultant failure rate is based on full utilization of device features under these specific conditions

Validation Study

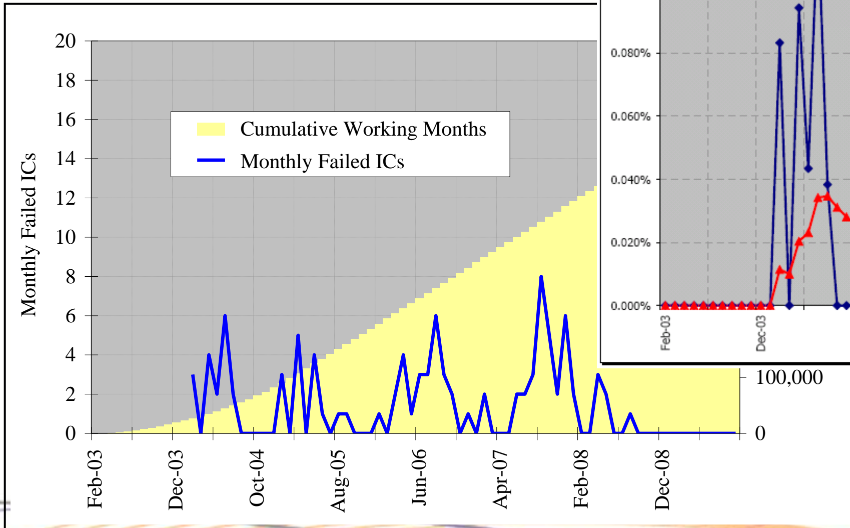
- Motorola field return data was gathered from family of telecommunication products
  - 56 different ICs comprised 41.5% of the failed part population
- The validation activity was utilized failure data from 5 integrated circuits

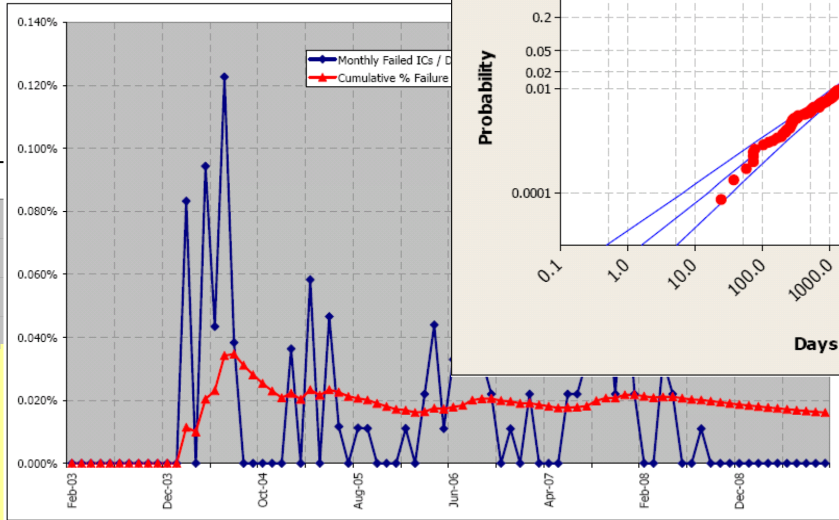


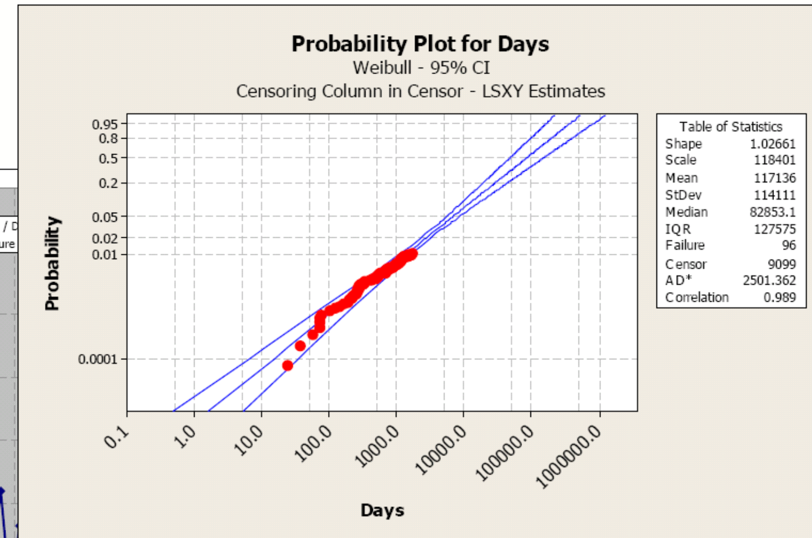
MFG	MFG Part Number	Year	Description	Quantity Replaced
HYNIX	HYMD512M646BF8-J	2004	1GB, DDRAM, MW800	190
MICRON	MT16LSDF3264HG-10EE4	2001	IC,SDRAM,2048MB,32M X 64,DIMM144,64MSRFRSH,MAX SUPPLY VOL 3.6V	152
SAMSUNG	M470L6524DU0-CB3	2005	DDR SDRAM SODDIM 512MB	161
FREESCALE	MC68HC908SR12CFA	2002	IC,MICROCONTROLLER,MC68HC908SR12CFA,,LQFP48,,,,512BYTE,,,12288BYTE	114
INTEL	RH80536GC0332MS L7EN	2005	IC,MICROPROCESSOR,SM,PENTIUM,1800MHZ,32BITS,2097152BYTE	18

Statistical Analysis on Field Returns

- Failure rate was calculated from raw data
  - Environmental conditions to determine in-field operating temperature
  - Thermal measurements to determine power dissipation
  - Cumulative failure distributions
    - Weibull
    - Exponential







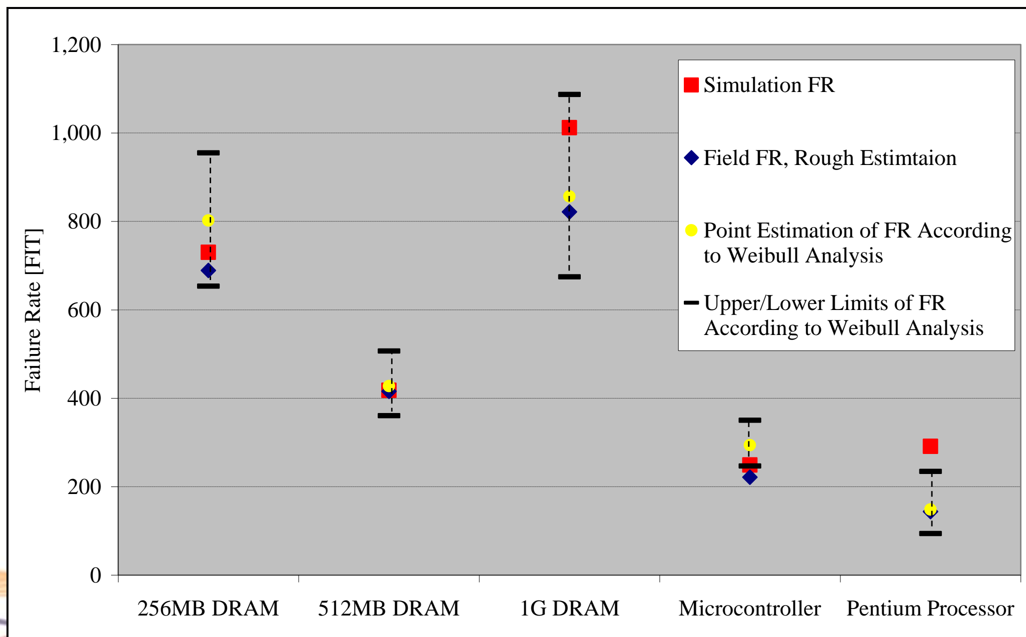
Extracted graphs from statistical analysis of field returns

Lifetime Prediction

Component Information:

Part Number	Description	Vendor	Node Technology	Field Temp. (C)	Calculated Test Temp. (C)	Vdd Field (V)	Vdd Test (V)
MT16LSDF3264HG-10EE4	256MB DRAM	Micron	150 nm	42	62.28	3	3.3
M470L6524DU0-CB3	512MB DRAM	Samsung	100 nm	42	70.00	2.5	2.7
HYMD512M646BF8-J	1GB DRAM	Hynix	110 nm	42	66.68	2.6	2.7
MC68HC908SR12CFA	Microcontroller	Motorola/ Freescale	90 nm	40	77.40	5	5.5
RH80536GC0332MSL7EN	Pentium Processor	Intel	90 nm	58	99.70	1.276	1.34

Failure rates and limits



Comparison of Results – JEDEC 47D HTOL

- Typical High Temperature Operating Life (HTOL) Test
  - Stated purpose is to simulate many years of operation at ambient, by testing at elevated temperatures and voltages
  - Test 77 pieces/qualification lot for 1000 hrs at 125°C (junction)
  - Zero failures
- Acceleration Factor
  - Accelerate via Arrhenius model with E_a=0.7 eV
- Result
  - For 3 lots (231 pcs) and operating temp of 55°C, the field operating time is ~18 million hours. At 60% confidence, *the failure rate is 51 FITs*

P/N	Field	Calculated	HTOL
256MB DRAM	689	730	51
512MB DRAM	415	418	51
IGB DRAM	821	1012	51
microcontroller	220	249	51
microprocessor	144	291	51

Comparison of Results – Parts Count MTBF

- Telcordia TR-322: Reliability Prediction Procedure for Electronic Equipment
  - Last Revision: Issue 6, December 1997
  - Replaced by SR-322, September 2006
- MIL-HDBK-217F (Notice 2): Reliability Prediction of Electronic Equipment
  - Last Revision: February 28, 1995 (per DoD repository)

Part Number	Field Failure Rate	Predicted Failure Rate	TR 322*	MIL 217F(2)*
MT16LSDF3264HG	689	730	15.4	18.6
M470L6524DU0	415	418	15.4	18.6
HYMD512M646BF8	821	1012	15.4	18.6
MC68HC908SR12CFA	220	249	27.0	18.1
RH80536GC0332MSL7EN	144	291	67.5	2691.3

*TR-322 and MIL-217-F(2) calculations performed using ALD Ltd. MTBF Calculator.

Application of Results

- Industry Standards
  - *VITA 51.2, Physics of Failure Reliability Predictions*
  - *MIL-HDBK-217J, Reliability Prediction of Electronic Systems*
    - *Addition of Physics-of-Failure requirements*
  - *IEC TS 62239, Preparation of an Electronic Component Management Plan*
    - *Addition of a wearout requirement*
- Certification requirements
  - *ARP 4761*
  - *ARP 5890*
- Platform customer requirements

Where Can We Go From Here?

- Future roadmap of existing features:
  - 65nm, 45nm, 32nm, 22nm technologies
  - Additional functional groups
    - Digital including logic and conditioners (e.g. gates)
    - Analog for signal processing (e.g. opamps)
    - Processor based (DSP, FPGA, etc)
- Customizable equivalent circuits and automated functional group analysis for ASIC design
- “Expert mode”
  - Modification of all default parameters
- Tradeoff analysis
  - Performance vs. Reliability

Questions?

- Q & A
- Would you like additional information?
  - Contact:

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