EPIDEMIOLOGICAL STUDY ON SN-AG-CU SOLDER: BENCHMARKING RESULTS FROM ACCELERATED LIFE TESTING

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ABSTRACT
This paper will present the results of a comprehensive overview of accelerated life testing (ALT) of components assembled with SnAgCu solder. Over 100 private documents and published articles were assessed for data on SnAgCu performance under temperature cycling. Data on test parameters, component materials and design, and interconnect dimensions were acquired and results were grouped by attach geometry, including leadless (i.e., Chip Resistors), stiff lead (i.e., Alloy 42), and solder ball (i.e., CSP, BGA). A particular emphasis was placed on obtaining temperature cycling data over a wide range of dwell times (5 to 360 minutes). Discussions will focus on trends in performance and will provide organizations that design, manufacture, or use Pb-free products first-pass expectations of times to failure under standard industry and military test specifications.

Key words: SnAgCu, SAC, Pb-free, leadfree, chip resistor, 2512, 1206, thin scale outline package, TSOP, Alloy 42, chip scale package, CSP, ball grid array, BGA, temperature cycling, dwell time

INTRODUCTION
Epidemiology is defined as the scientific study of factors affecting the health of various populations. The purpose of an epidemiological study is to predict the behavior/survivability when a particular population is subjected to stressful conditions (environment, disease, etc.). With the recent transition of consumer/commercial products to Pb-free solder and the growing consideration of Pb-free solder for applications with high-reliability requirements (industrial controls, avionics, military), there is a critical need to collate and review the results of existing reliability studies with the end result providing expectations of time to failure under standard accelerated test conditions.

A ‘test-to-spec’ approach, where units are subjected to standard industry/military test specifications and no failures are expected, is not best practice in ensuring long-term reliability of electronics. For each new technology, new design or new operating environment, a reliability assessment using validated physics of failure (PoF) based models [1-3] should be performed. This assessment would be performed for a realistic worst-case field environment and the accelerated test environment and the end result would be two time-to-failure predictions. The resulting ratio of time-to-failure in the field over time-to-failure during test provides an acceleration factor. This acceleration factor can then be used to design a life test with optimum efficiency. The product would then experience the same level of stresses expected over the design life and the risk of understressing the design or inducing irrelevant failures would effectively drop to zero.

Unfortunately, the reality of the electronics industry is that once a product qualification schedule is developed by internal quality/reliability personnel, modifications in regards to the type of testing or test parameters are rarely performed. This inertia often results in a surprising amount of consternation and delay in product release when failures are detected during testing. The major motivation for this paper therefore was to avoid this scenario by allowing quality/reliability engineers/technicians to review the design and the planned accelerated life test (ALT) and to quickly determine if there is a reasonable risk that a Pb-free product may experience failure. If failure may occur, PoF models for Pb-free solders could then be used to confirm sufficient design life in the actual operating environment.

DATA GATHERING
The primary focus during data gathering was time to failure data for Pb-free solder under a variety of standard test conditions. Time to failure data was categorized as two-parameter Weibull. Characteristic life (eta, time to 63% failure) was obtained either directly from the publication or derived from the raw data using Weibull++ (Reliasoft, Phoenix, AZ). The shape parameter (beta) was also obtained when available.

While a universal Pb-free solder has yet to be established, and may be unobtainable given the increasing interest in SnNiCuX and SACX alloys, for greatest relevance the Pb-free solder for this epidemiological study was limited to the tin-copper-silver (SnAgCu) family. Specifically, a formulation range of 4.0wt% to 3.0wt% Ag and 0.9wt% to 0.5wt% Cu. The choice of alloy and composition was based on its dominance in the industry over the past five years and evidence from an IPC study that time to failure behavior over this range was relatively consistent [4].

Attempts to limit data collection to standard test conditions was not an issue as even academic and research institutions almost exclusively perform testing in correlation with industry/military specifications. The majority of data was obtained from thermal cycling testing, most likely because

this is the primary environmental stress for the consumer/computer applications that initially transitioned to Pb-free.

While numerous components have been subjected to a variety of accelerated life tests, the focus of this study was to identify and catalogue the behavior of common components that are the most susceptible to failure during product qualification. These were identified as

- Chip resistors (1206 and 2512 case sizes)
- Thin scale outline packages (TSOP) with Alloy 42 leadframe
- Area array devices (ball grid array and chip scale packages)

Attempts to extract additional information, especially in regards to developing validation data for PoF models, was limited by the lack of a standard format for reporting reliability data. Numerous publications failed to report the most basic of information, including component size, die size, dwell times, ramp rates, board coefficient of thermal expansion (CTE), or other important design or materials information. Almost all the publications failed to provide details on the solder volume, such as board bond pad dimensions, stencil thickness, or solder joint height. In addition, relevant procedural information, such as monitoring or event detection, number of samples tested, number of samples failed, and validation that failures were not at other locations (such as vias), was often not provided in sufficient detail.

This absence of data can be critical, as all predictive models for long-term reliability of SnAgCu solder depend on test results to validate their output. Lack of reliable data can result in a lack of reliable end-of-life models and should drive professional organizations, such as SMTA, IEEE, IPC, and IMAPS, to consider a global specification on required data formats when reporting the results of reliability testing.

The second limitation was the lack of repeatability. Repeatability and reproducibility (R&R) have become a standard practice in manufacturing to ensure a sufficient level of quality control. While the cost and time associated with temperature cycling to failure can definitively hinder the implementation of R&R, it should be strongly considered as a review of the literature seems to identify several examples of outliers that show very poor correlation with test results from other publications and may not be repeatable.

TEMPERATURE CYCLING

Use of temperature cycling is the most common test condition for product qualification. Heavy reliance on older military specifications has resulted in a common set of test parameters, including temperature range, dwell time, and ramp rates. This standardization facilitated analysis and observations of behavior trends. Severe temperature deltas are the most common accelerated life tests and primarily consist of the following:

- -55C to 125C
- -40C to 125C
- 0C to 100C

Surprisingly, this investigation found relatively few examples of -40 to 85C testing on Pb-free assemblies, even though this corresponds to an industrially rated component.

Some examples of severe test conditions with a maximum temperature of 150C were also identified. These extreme conditions, minimum temperatures below -40C and maximum temperatures above 125C, are often justified for the applicability to the use environment (e.g., under the hood). However, a broad review of test results under extreme environments and comparison to the more standard -40C to 125C suggests that these environments do not result in fewer cycles to failure.

More benign conditions, such as 40 to 100C, were less common, but were critical for extrapolation of behaviors to conditions more representative of field conditions.

Standardization, and the need for time efficiency, has also resulted in a limited range in dwell times of 5 to 15 minutes. Because of the increasing popularity of thermal shock testing, there is a much broader range in ramp rates, from 4C/min to 200C/min (claims of ramp rates greater than 200C/min are unrealistic due to heat transfer and heat capacity limitations). However, recent work demonstrated that ramp rates tend to have a negligible or secondary effect when compared to other environmental and component parameters [3].

Comparing the information retrieved from the various papers can be difficult as a number of experimental designs were setup to assess the influence of parameters separate from the component, interconnect or environment. For example, the dataset from Woodrow [6] included varying the Pb-free solderability plating between immersion silver (ImAg), organic solderability preservative (OSP), and electroless nickel/immersion gold (ENIG). A similar effort was made by Schubert [14]. Other non-environmental drivers investigated included cooling rates [10] and the number of reflows [13]. In addition, some experimental coupons consisted of test boards with thicknesses less than 60 mil. For medium to large components, a thinner board introduces additional compliance into the test system, resulting in a non-pertinent extension in time to failure.

Leadless / Stiff Lead

Two packaging styles most susceptible to failures during temperature cycling are leadless components and components with stiff leadframes (e.g., Alloy42 leadframe). These components also tend to provide a narrower spreader of failure data and easier trend spotting because there is minimal variation in packaging materials or geometry.

Characteristic life as a function of change in temperature, ΔT, for leadless chip resistors and TSOPs with Alloy42

leadframes are displayed in Figure 1 and Figure 2, respectively. While data was obtained for both 1206 (120 mil length by 60 mil width) and 2512 (250 mil length by 120 mil width) case sizes, the lack of test data at below -40C to 125C for the 1206 case size limited extrapolation to the 2512 case size.

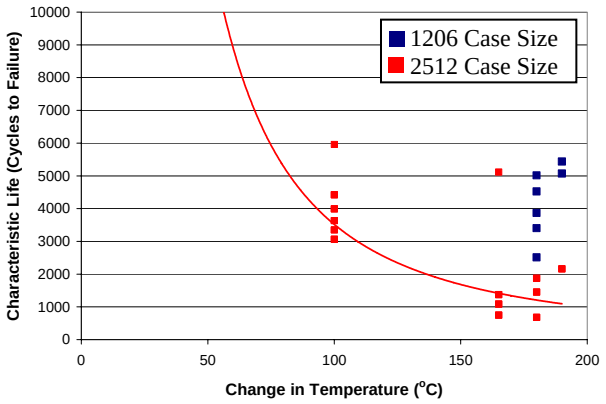

Figure 1: Cycles to failure as a function of change in temperature during thermal cycling for leadless chip resistors attached with SAC solder.

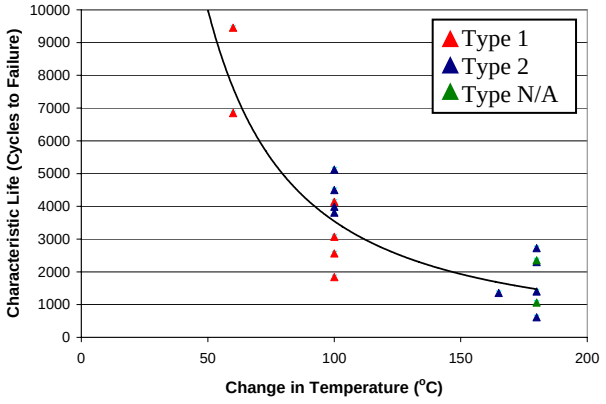

Figure 2: Cycles to failure as a function of change in temperature during thermal cycling for TSOPs with Alloy42 leadframe attached with SAC solder.

An initial review of the data identified several interesting findings.

- The time to failure behaviors for 2512 resistors and Alloy 42 TSOPs are very similar
- For both 2512 and TSOP, cycles to failure displayed a power law dependence (-1.5) to ΔT. This conforms to findings from previous studies
- For Alloy 42 TSOPs, time to failure seemed to be relatively independent number of I/O (44 to 56 leads) or package design (Type 1 or Type 2)(see Figure 3)

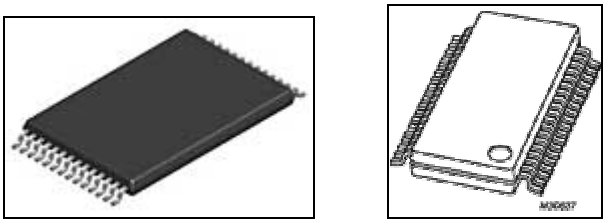

Figure 3: Type 1 and Type 2 TSOP package styles.

Characteristic life, however, is not a particularly valid point of reference for product qualification as very few organizations are willing to test product until 63.2% fail. A more relevant parameter would be to identify when wearout could initiate given the relatively low number of samples often subjected to product qualification (anywhere from 3 to 77). Given the low number of samples and the low degree of confidence in extrapolations to 1%, a more relevant prediction of first failure would be based on cycles to 10% failure.

Weibull plots for cycles to failure for 2512 resistors and Alloy42 TSOPs are displayed in Figure 4 and Figure 5, respectively. The shape parameter, beta, allows for extrapolation back from the characteristic life to time to 10% failure. The average shape parameter for 2512 resistors was 3.3, with a reported range of 1.7 to 5.6. The average shape parameter for Alloy 42 TSOPs was slightly higher, 7.7, with a broader range of 2.7 to 22. Based on these Weibull characteristics, a realistic expectation of first failure during product qualification is displayed in Table 1.

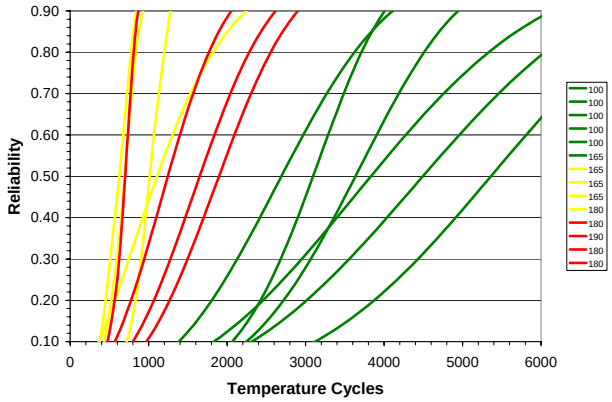

Figure 4: Two parameter Weibull plots of 2512 resistors attached using SAC solder and subjected to various temperature cycles (0C to 100C: 100; -40C to 125C: 165; -55C to 125C: 180).

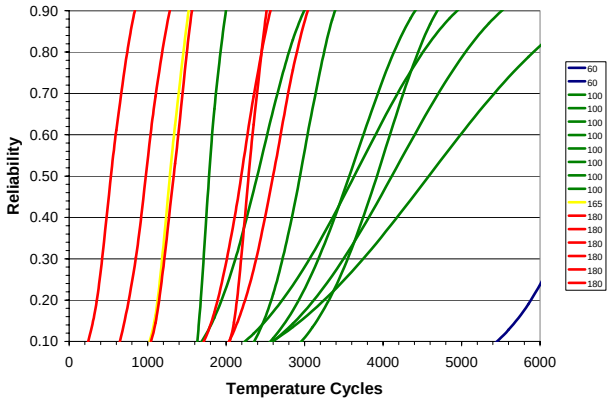

Figure 5: Two parameter Weibull plots of Alloy42 TSOPs attached using SAC solder and subjected to various temperature cycles (40C to 100C: 60; 0C to 100C: 100; -40C to 125C: 165; -55C to 125C: 180).

An alternate way to read Table 1 is that Pb-free designs containing either 2512 chip resistors or Alloy42 TSOPs should not be expected to survive more than 500 cycles of -40C to 125C or 1500 cycles of 0C to 100C. Internal specifications that call out a higher number of cycles will likely induce failure during product qualification and these failures will be due to inherent design limitations. On the other hand, if failures are observed significantly earlier than the specified number of cycles, this would strongly suggest the presence of manufacturing defects.

Table 1: Estimated cycles to first failure during product qualification

	Temperature Cycle	
Package	**0C to 100C**	**-40C to 125C**
2512	1500 cycles	500 cycles
TSOP	1500 cycles	500 cycles

Area Array

The other packaging style of concern during temperature cycling are those with area array interconnects. This primarily consists of ball grid arrays (BGAs) and chip scale packages (CSPs). The point of differentiation between BGAs and CSPs is not always well defined other than CSPs contain a die that is 80% or greater than the total area of the package. As a general statement, CSPs tend to be smaller, have fewer I/O, and have a finer pitch. However, since this study categorized based on authors' descriptions, there was some overlap in terms of number of I/O (144 pin BGA; 169 pin CSP) and pitch (0.65 mm pitch BGA; 0.8 mm pitch CSP).

Characteristic life as a function of ΔT for plastic BGAs (PBGAs), flex and ceramic BGAs, and CSPs are displayed in Figure 6, Figure 7, and Figure 8, respectively. All the data from CSPs were on non-underfilled packages. The average shape parameter was found to be approximately 9.7 for BGAs and 6.2 for CSPs with both package styles having a very broad range of reported values (2.5 to 30).

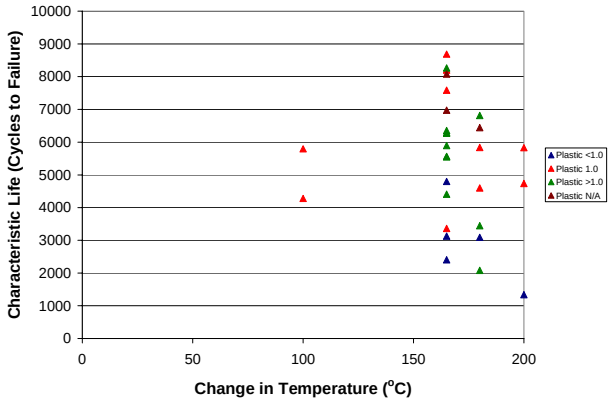

Figure 6: Cycles to failure as a function of change in temperature during thermal cycling for PBGAs attached with SAC solder. Coloration identifies different pitches (less than 1.0 mm, 1.0 mm, greater than 1.0 mm, unknown).

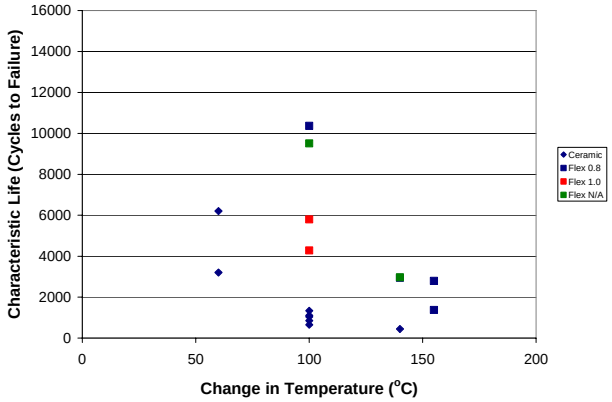

Figure 7: Cycles to failure as a function of change in temperature during thermal cycling for ceramic and flex BGAs attached with SAC solder. Coloration identifies different pitches (0.8 mm, 1.0 mm, unknown).

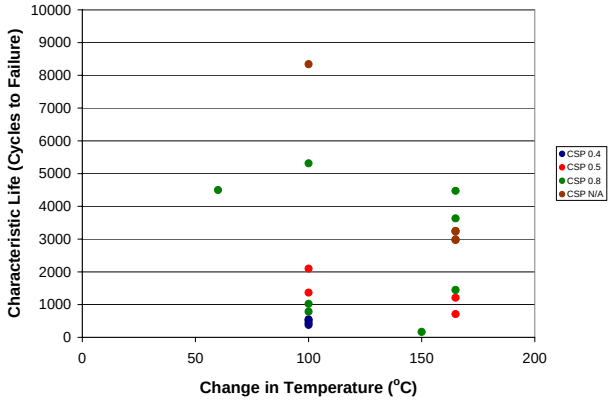

Figure 8: Cycles to failure as a function of change in temperature during thermal cycling for CSPs attached with SAC solder. Coloration identifies different pitches (0.4 mm, 0.5 mm, 0.8 mm, unknown).

While the range in cycles to failure is much greater than observed with 2512 resistors or Alloy42 TSOPs, it is interesting to note that the range is still within the claimed accuracy of most physics of failure based models of 2X. For example, a PBGA experiences failure after 4500 cycles of -40C to 125C. A reliability model would be considered to be relatively accurate if it predicted time to failure between 2250 cycles and 9000 cycles. This is within the observable range of all SAC solder PBGAs tested within the reportable literature.

The range of cycle to failure date for CSPs was especially disappointing as it would be assumed that the die characteristics (coefficient of thermal expansion, elastic modulus) would dominate behavior and time to failure could segregated by package, and thus die, dimensions. The lack of correlation signals the strong influence of the interposer material and design in ensuring reliability.

Since area array package design and materials are less standardized, and thus lead to a wider range of potential failure behavior, any observation of behavior trends requires tracking only those datasets that contain at least two temperature cycles. The characteristic life for these datasets was normalized around the 0C to 100C thermal cycle and the results are displayed in Figure 9.

The area array devices were found to also display a power law behavior in response to changes in ΔT, but the best fit exponent is -2.7, as opposed to -1.5 for the 2512 resistor and Alloy42 TSOP.

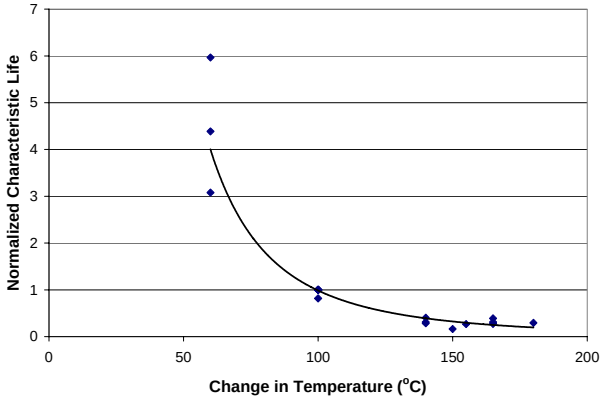

Figure 9: Normalized characteristic lifetime as a function of change in temperature for area array packages (BGAs and CSPs)

Dwell Time

While there is an understanding within the reliability community that the failure behavior of SAC solder is very dependent upon dwell time, surprisingly few experimental data points exist on the influence of long-term dwells on time to failure during temperature cycling. Only three publications have reported on the influence of dwell times greater than 30 minutes (Bartello, Henshall, Bath) and all three publications relied on a 0C to 100C thermal cycle. Due to this extremely limited dataset, the influence of long-term dwell was also assessed using results from finite element analysis of a 2512 chip resistor subjected to 25C to 80C temperature cycling. Cycles to failure were calculated based on creep behavior derived from Schubert and a damage model from Syed (Blattau). Data from the four experimental and one modeling results were normalized by cycles to failure for a 10 minute dwell. The results are displayed in Figure 10.

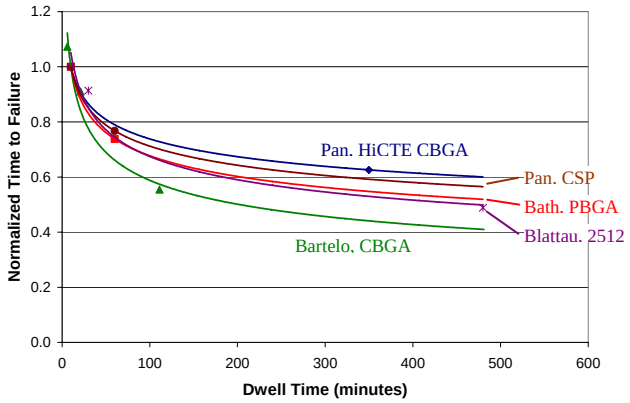

Figure 10: Normalized time to failure as a function of dwell time at maximum temperature for SAC solder.

Figure 10 demonstrates, as would be expected, that lower temperatures and smaller differences in coefficient of thermal expansion (CTE) reduce the influence of dwell time on failure behavior. Under a worst-case scenario, such as a large ceramic ball grid array reaching 100C, time to failure in the field (8 hour dwell) could be as much as 60% less than time to failure under test (10 minute dwell). However, under more benign conditions, such as a plastic ball grid array with a maximum temperature of 80C, extended dwells may only reduce time to failure by 25-30%.

SAC vs. SnPb

The initial purpose of this study was not to compare the reliability of SAC and SnPb connections, especially in regards to field performance. A more appropriate methodology for this analysis would be to use physics of failure based reliability models. However, the plotting of SAC behavior over long-term dwells in Figure 10 does provide the ability to provide a more relevant comparison than has been offered in standard accelerated life tests.

Relevant time to failure comparisons require incorporation of the effect of long-term dwell and extrapolation of time to 1% failure, as opposed to characteristic life. These influences were taken into consideration and are plotted in Figure 11 and Figure 12. In each figure, the influence of long-term dwells (8 hours) on SAC behavior was plotted as reducing time to failure to 75% (nominal) and 50% (worst-case) of short-term dwells (10 minutes).

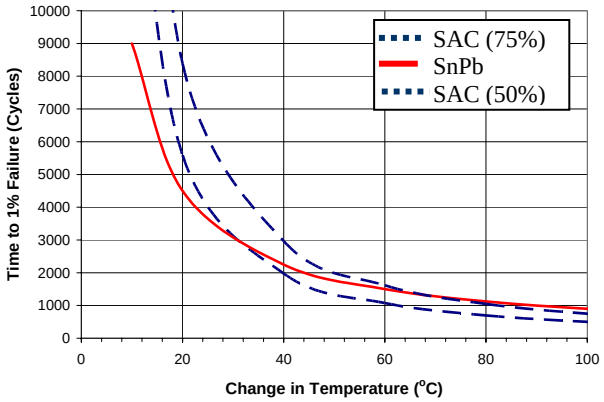

Figure 11: Time to 1% failure for 2512 resistors attached with SAC or SnPb solder and subjected to long dwells (~8 hours).

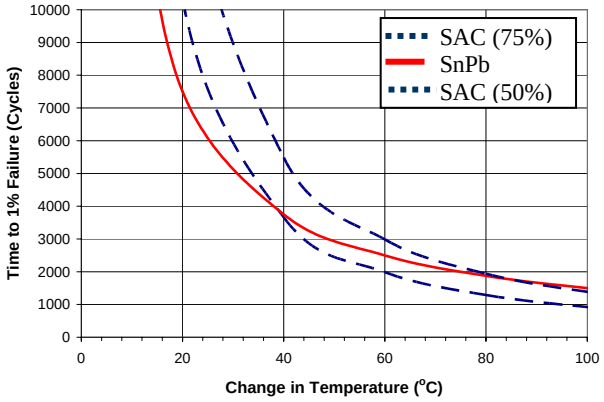

Figure 12: Time to 1% failure for Alloy42 TSOPs attached with SAC or SnPb solder and subjected to long dwells (~8 hours).

It can be seen that the superior robustness observed with SAC during accelerated life testing is for most part eliminated when the lower beta and degradation during long-term dwells is considered. Given the expected confidence bounds and degree of uncertainty, it is not unrealistic to state that the field failure behavior of SAC and SnPb assemblies will be roughly equivalent.

Because of the wide variation in BGA/CSP design and materials, a similar direct comparison using accelerated life test data is not possible. However, as with Figure 9, a relative comparison of SAC vs. SnPb reliability can be performed. The ratio of SAC lifetime vs SnPb lifetime as a function of ΔT for area array devices is displayed in Figure 13 and Figure 14.

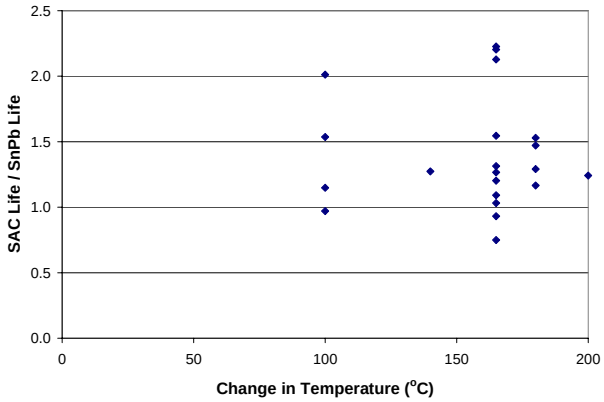

Figure 13: Ratio of SAC/SnPb reliability for area array devices as a function of change in temperature.

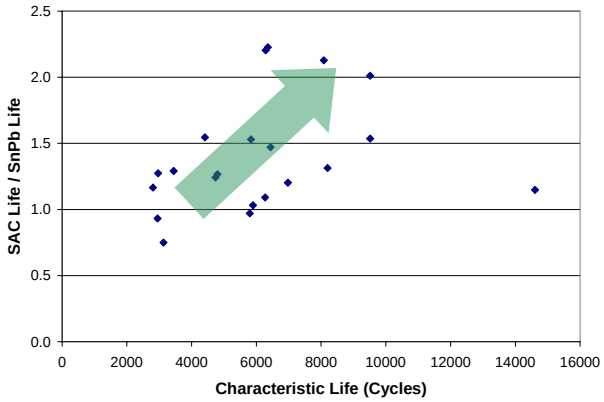

Figure 14: Ratio of SAC/SnPb reliability for area array devices as a function of characteristic lifetime of the SAC component.

While there is no obvious one-to-one influence of ΔT on SAC/SnPb ratio, the green arrow in Figure 14 marks a general increase in SAC's reliability over SnPb as the time to failure increases. Again, this makes sense based upon the existing industry knowledge base. Lower maximum temperatures and smaller mismatches in CTE result in an increase in time to failure and reduce the creep constituent in the damage evolution in SAC.

However, a different trend arises if we take into account the effect of long-term dwell (25% reduction in life) and extrapolate to 1% failure behavior. As shown in Figure 15 and ignoring obvious outliers, the ratio of SAC-to-SnPb reliability seems to be relatively independent of time to failure and in general shows a slight less than 1:1 ratio.

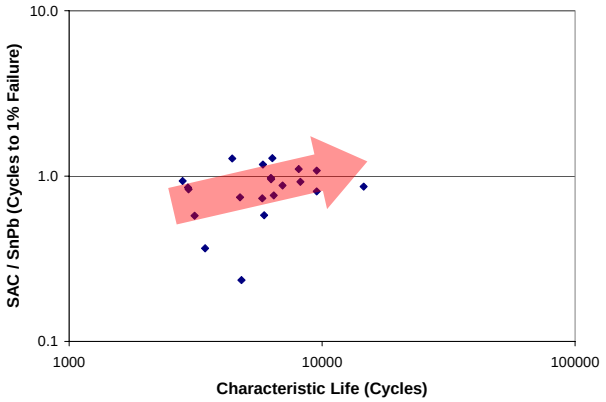

Figure 15: Ratio of SAC/SnPb time to 1% failure for area array devices as a function of characteristic lifetime of the SAC component and taking into account long-term dwell (8 hours).

VIBRATION

There is currently an ongoing effort to complete an epidemiological study on the performance of SAC solder under vibration. While this effort is more complex due to the wide range of test conditions and package geometries selected for vibration testing, initial indications seem to suggest similar performance to SnPb.

MECHANICAL SHOCK

There is currently an ongoing effort to complete an epidemiological study on the performance of SAC solder under vibration, both with and without preconditioning consisting of long-term aging. While a variety of package styles are subjected to mechanical shock, the recent adoption of an industry standard, JESD22-B111 [47], allows for the stronger likelihood of identification of definitive trends.

CONCLUSION

As a result of extensive data gathering and analysis, several important conclusions regarding SAC reliability were obtained:

- As a general observation, testing at temperatures higher than 125C or lower than -40C does not result in significantly fewer cycles to failure
- 2512 chip resistors and TSOPs with Alloy42 leadframes can not be expected to survive more than 500 cycles of -40C to 125C and 1500 cycles of 0C to 100C
- Leadless and stiff leaded components display a -1.5 power law dependence on ΔT while area array components display a -2.7 power law behavior
- The effect of long-term dwell, up to 8 hours, would be expected to reduce lifetime by 40 to 60% during testing and 25 to 40% during field use
- Once long-term dwell and differences in shape parameters are taken into account, there is likely to be no statistically measurable difference in time to failure for SAC and SnPb assemblies over most operating environments

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