Failure Analysis of Electrostatic Discharge and Electrical Overstress Failures of GaAs MMIC

Yu-chul Hwang, Mikyoung Lee, and Michael Pecht
CALCE Electronic Products and Systems Center
University of Maryland
College Park MD 20742

Abstract

Failure mode and effect analysis, visual inspection, electrical tests, X-ray observation, optical microscopy and scanning electron microscopy were performed on failed linear GaAs MMIC voltage variable absorptive attenuators. Human body model electrostatic discharge tests and electrical overstress tests were performed to replicate the failures. The studies showed that the failure locations and damage shapes varied depending upon how the failures were replicated. Failure analysis results between the replicated failures and the field failures were compared. From the extent of damage and its shape on the field failure and replicate tests, it appears that field failure was caused by ESD stresses.

Keywords: GaAs MMIC, ESD, EOS, HBM, failure analysis

Introduction

As IC device density increases, devices are becoming increasingly susceptible to Electro Static Discharge (ESD) damage. ESD's short, fast and high-amplitude pulses are an inevitable part of the day-to-day environment of both devices and equipments. The Quality and Reliability Council of Sematech has ranked ESD as the second most important cause to affect the yield and reliability of integrated circuits[1] [1].

Electrical Over Stress (EOS) is commonly the most frequently occurring failure mode in semiconductor devices of all types. ESD is actually a subset of the more general range of failures associated with EOS. However, EOS is generally associated with over voltage and over- current stress of long time durations, usually associated with events, which occur during normal circuit operation, screening or test conditions.

Gallium Arsenide Monolithic Microwave ICs (MMIC) contain planar transmission lines, distributed elements, and active devices on the same substrate. Planar structures on GaAs are based on various types of metal films as required for Ohmic and Schottky contacts. Unlike silicon-based technology, GaAs devices have no dielectric oxide layer due to their semi-insulating nature. Gold and gold-based alloys such as AuGeNi are used for metallization on GaAs [2].

MMICs are commonly used in telecommunication products, TV receivers for satellite broadcasting, and in radar and navigation systems. MMIC devices are considered equivalent to a circuit having multiple paths to the ground. If one pin is grounded, then electric potentials sufficient to cause dielectric breakdown may be discharged through the device. This electrostatic discharge can damage the gate metallization in GaAs substrates causing cracking of the device gate metal or localized melting. Melting of small amounts of the device metal lines create minute explosion-like effects on the device surface such as voids, cratering and subsequent short circuit or open circuit.

Experimental Approach

The human body model pulse test, one of three commonly used ESD test standards [3],[4],[5], simulates the current discharged from a human's touching an IC, when there is a potential between the human and the IC. ESD test standards help assure consistency and also provide a means of objective evaluation and comparison. Often this kind of potential difference builds up due to triboelectric charging. The ESD event can often occur by inadvertent handling.

Since there is no specific standard for EOS, it has been applied with specific excessive voltages. The voltage of test was increased step by step until it showed electrical malfunctions such as open or short. Prior to ESD or

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[1]Number one problem is electromigration.

EOS characterizations, complete DC parameter and functional testing per applicable device specification requirement was performed on all test devices. Known good devices were subjected to a DC voltage applied between pins.

Once ESD and EOS testing were completed, failure characteristics following failure analysis process in Figure 1 were analyzed with the help of various identification methods for failure location and damage shape. It starts with visual inspection for anomaly, electrical test of the performance, and X-ray, optical microscopy and SEM for locating the defect. Liquid crystal or Infrared thermal tracer observation is also considered to implement in order to indicate failure sites which are not found by optical microscopy or scanning electron microscopy (SEM) [6].

(1) ESD Simulation

There are three common ESD test models for ESD failure identification [3],[4],[5]. When a charged human body touches an IC (Human Body Model), a charged IC touches a grounded surface (Charged Device Model), and when a charged machine touches an IC (Machine Model) so an electrostatic field induces a voltage across a dielectric or gate oxide or metallization that is sufficient to break it down. In this study, HBM test was performed with 3 unused (good) devices. The devices were no power applied during ESD testing.
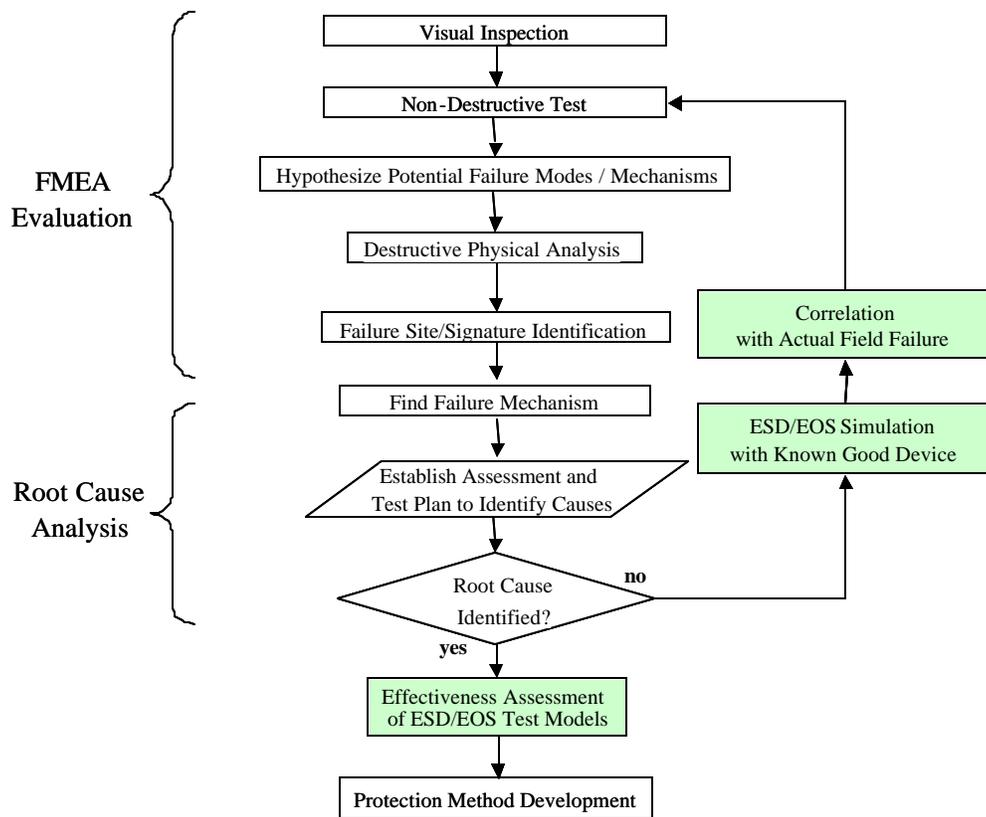

Figure 1. Flowchart for the failure analysis process

(2) EOS Test

In order to analyze the failures associated with electrical overstress (EOS), four unused (good) devices were subjected to a DC voltage applied between V_{cc} (pin4) and ground and V_c (pin5) and ground. Electrical characteristics of the devices were analyzed by I-V curve tracer after EOS test. The voltage level was increased in steps of 5V, until the devices exhibit electrical malfunctions. No other power was supplied to devices during EOS test and all other pins were floating.

Because EOS current could enter into any pin and go out from another pin of an IC, to practically verify the sensitivity of whole IC on EOS, additional EOS conditions have to be considered. With additional voltage simultaneously applied to V_c pin, the devices showed short or open circuits at $20V(V_c)$ and $40V(V_{cc})$. Test condition 2 showed another combination of voltages that failed devices. Voltage level applied to V_c was increased by 5V until the devices failed.

Failure Analysis

Total fourteen devices were subjected to failure analysis. It includes three ESD-stressed devices, four EOS-stressed devices, 5 burn-screen failed devices and two known good devices. Through comparison with each other, the root cause can be found if ESD or EOS caused burn-in failures.

(1) Visual Inspection

The external conditions of failed devices were inspected by stereomicroscope for package related anomalies. No anomalies were observed on any of the devices.

(2) I-V Trace and Characteristic Performance Check

The analysis involved running a DC analysis on ESD / EOS stressed devices, burn-in failed devices and known good devices to check for short and open at the RF terminals with IV curve. The path from RF_{in} to RF_{out} goes through the gate diodes in FET. A short of either diode D_1 or D_2 produces an abnormal curve shape. The path from Vc to RF_{in} or RF_{out} goes through either diode D_1 or D_2 and resistance R_1. A short across R_1 produces a decrease in the resistance and trace curve will be closer to vertical line while a open in R_1 increases the resistance and closer to horizontal line. The failure criterion in this study is the change of current-voltage (I-V) characteristics at the input and output terminals.

In the ESD test, stressed device showed resistivity short. In EOS tests, three out of four stressed devices showed resistivity short and one showed resistivity open between RF and Vc pin. As results of electrical characteristics check, there existed two types of failure modes according to applied EOS/ESD stress, electrical short or open. For five burn-in failed devices, three of them showed resistivity short while two showed resistivity open.

(3) X-Ray Observation

X-Ray observation was performed to nondestructively examine the ICs gross internal anomalies such as wire bond failure and die cracking. ESD/EOS stressed and burned-in failed devices showed no defects.

(4) Decapsulation and Optical Microscopy Observation

Internal visual inspection of the die and bond wires was carried out at various magnifications. The device of normal characteristics was also decapsulated for visual comparison. ESD stressed device shows an anomaly near RF_{out}, which gives electrical short between RF_{out} and Vc. EOS stressed devices revealed comparatively large anomalies on the die surface. The electrical short located near a gate channel of the device exists. In addition, damage was located at the RF input resistor locations. For failed devices from both test condition 1 and 2, failure mode was same but failure locations on die surfaces and size and shape of failure signatures were quite different from each other. Test condition 1 burned the die surface completely. For devices from test condition 2, failure mode was electrical short between RF_{in} pin and Vc pin, which was the same as that of ESD tested devices, but location and size of failure were quite different. With test condition 2, metallization layer of failure site was melted at around Vc pin, and size of melted area was much bigger than that of ESD failure

The system level burn-in failed device revealed a visual anomaly in a unit. The electrical short located near a gate channel of the device was found. In addition, damage was located at the RF_{in} resistor (R_1) locations. Electrical probing indicated that the RF_{in} FET is a resistive short. The terminals of the affected resistor are directly connected to pin 5 (V_c), while they are indirectly connected to pin3 (RF_{in}) and 7 (RF_{out}).

(5) Environmental Scanning Electron Microscopy (E-SEM) observation

E-SEM of field-failed device revealed an anomaly. A circle with an arrow shows the structural damage located near a gate channel of the die surface. This damage causes an electrical short and appears to be the same

shape that ESD induced. This surface breakdown can occur when the voltage is high enough to bridge a gap between two metal lines, on the device surface, which is called gaseous arc breakdown.

Discussion and Conclusions

A microelectronic part level and system level burn-in screening performed to precipitate defects by exposing the parts to accelerated stress levels. The goal of this screening is to prevent failures from occurring in the field. Burn-in process commonly consists of placing parts in a thermal chamber for a specific amount of time under an electrical bias. During and/or after thermal environmental exposure, functional tests are conducted. The temperature applied during burn-in is higher than the temperature the part will encounter in the field, as a perceived means of reducing the time to precipitate defects. Other accelerated conditions, which may be a part of the burn-in process, include voltage, humidity, electric field, and current density [7].

Though burn-in is focused on reducing the early failure and maximizing the mean time to failure, as the reliability of microelectronic part improves, burn-in may cause other additional failures during preparation and handling process rather than remove failures. So most of the burn-in tests are impractical or need modification for new technologies, and add little or no value for mature technologies.

Failures caused by burn-in process are mainly due to electrical overstress (EOS) and electrostatic discharge (ESD) damage. EOS is mainly caused by misapplied power and ESD is mainly caused by additional handling process during burn-in test. Burn-in test includes many dangerous processes in terms of ESD (socketing, moving, electrical test, and human and machine contact). As considering that ESD occurs from human touch, machine touch and charged device itself, these procedures provides the possibility that devices are exposed to certain conditions in which ESD events occur [8]. Moreover, it raises the issue of latent ESD damage in devices. This also shows that burn-in not only adds no value, but it may even increase the field failure rate of the devices [9].

In this study, the evidence of ESD/EOS failure in GaAs MMICs after system level burn-in screen was sought. It is premature to define the cause of burn-in failure even though there exists possibility due to ESD/EOS. The failure mode and signature of burn-in-failed devices and ESD and EOS tested devices were studied and photographed for comparison. The analysis of five devices that failed in burn-in showed two different electrical failure modes (three resistivity short devices and two resistivity open devices). The devices from HBM ESD simulation showed resistivity short in two devices. In the EOS test, there were three open and one short failures.

The ESD test result shows a different location of damage from the burn-in screen devices. The result of EOS test does not show similarity in damage shape and location to burn-in failed defects. Test results also revealed similarities in EOS / ESD and burn-in failure modes, so failure mode itself doesn't provide enough information to identify the root cause in this device.

An important difference between ESD and EOS damage is the size of the damage site. With ESD, a SEM must be used to view the damaged area, along with careful removal and etching of layers. With EOS damage, on the other hand, the area can be observed in a low power optical microscope.

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