Thermal & Electrical Performance and Reliability Results for Cavity-Up Enhanced BGAs

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Abstract

A new cavity-up enhanced flex-based BGA package, which adds an integral copper interposer between the die and the flex, expands the options available to the electronic industry for increasing reliability, thermal and electronic package performance, offering improvements compared with many prominent flex-based CSP and BGAs. For board-level reliability, CTE measurements of this enhanced BGA using a moiré fringe technique predicted thermal cycling performance similar to µBGA and superior to rigid organic laminates, ceramic CSPs and flex-only packages. Package-level reliability testing of the enhanced BGA has identified some common assembly die attach and overmold materials combinations that have performed to JEDEC Level 1 in moisture resistance tests. Thermal computational fluid dynamics (CFD) modeling of the enhanced BGA package with the interposer showed substantially lower junction temperatures in two application environments, as compared to the analogous flex-based package construction without the interposer. Electrical analysis using a boundary element electromagnetic field solver to extract fundamental electrical circuit parameters over a broad range of operating frequencies also predicted electrical performance benefits for the enhanced BGA with interposer versus the same construction without the interposer.

Introduction

With the popularity of portable electronics such as cellular phones, pagers, camcorders and laptop computers, the electronics industry has driven toward smaller solutions to electronic packaging. This miniaturization will continue with increasing electronic packaging performance and board level reliability. A new flex-based enhanced BGA package with cavity-up orientation addresses these strong market drivers.

Small form factor packages (including chip scale packages or CSPs) describe first-level electronic packaging where size is critical. Flex-based packaging, where a flexible circuit is the redistribution interconnection of the package, is fast becoming the chip scale packaging alternative of choice [1].

Package performance requirements remain stringent with respect to thermal dissipation, electrical signal inductance, to support increasing frequencies and silicon integration, and board level reliability, to meet the service life of the end product. Not all electronic market segments have adopted small form factor packages, primarily because of concerns about electronic package performance and less than desired board level reliability [2,3].

This paper describes the practical aspects of the electronic package performance and package reliability of prominent flex-based chip scale and BGA packages in contrast to a new flex-based enhanced BGA with cavity-up orientation for applications that include small form factor and demanding reliability, thermal and electrical performance.

Wire Bond Flex Construction

The highest volume flex-based package in production today is the wire bond flex BGA (known as µStar™ at Texas Instruments and *fle*XBGA™ at Amkor) [4]. This is a wire bonded, cavity-up construction with versatility for "fan-in" and "fan-out" options as shown in Figure 1. The main advantage of this package is its simplicity and potential low cost.

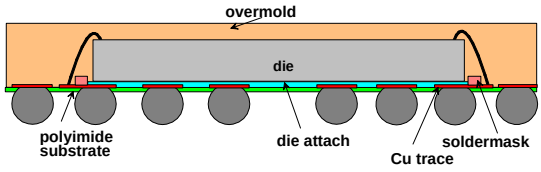


Figure 1. Wire bond flex BGA in a near CSP format (fan-in and fan-out).

µBGA® Package Construction

Tessera's µBGA is another recognized flex-based CSP construction. This is a TAB type, cavity down construction in a "fan-in" form as shown in Figure 2. The main advantage of this package is the compliant elastomer layer which isolates the shear strain caused by the thermal expansion mismatch between the silicon die and the circuit board substrate.

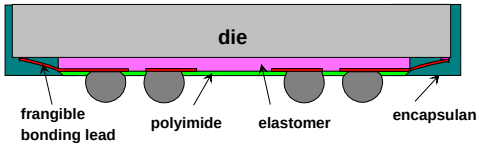


Figure 2. Tessera's µBGA package with "fan-in" ball pattern. The elastomer layer is used to absorb CTE mismatch strain.

Enhanced BGA Package Construction

This new cavity-up enhanced BGA package construction is similar to the wire bond flex BGA with the addition of a thin 5-mil copper interposer-stiffener laminated to the flex circuit in the manner shown in Figure 3. The stiffener component of the electronic package design enhances the package performance in terms of heat dissipation/spreading from the IC, electrical reference for signal integrity and matched CTE to FR4 to reduce solder ball strain.

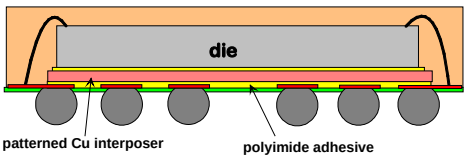


Figure 3. Enhanced BGA in a CSP format. The copper interposer enables a matched CTE to the printed circuit board.

This new package substrate consists of traditional 3M Microflex circuitry laminated to a metal stiffener-leadframe with a thermoplastic adhesive. The flexible circuit, as the redistribution interconnection of the package, takes advantage of the high resolution capability of flex and enables the routing of dense ball arrays thereby minimizing package size and metal wiring levels [5]. In addition to routability, the resolution capability of the flex circuit enables the wire bond pads to be positioned close to the die to enable minimization of both the die size and the package size. This finer pad pitch enables die shrink while maintaining relatively short bond wires to minimize self-inductance.

Figure 4 shows the package substrate as supplied by 3M to package assemblers who complete the IC package. The flex laminated to stiffener serves as a "leadframe" during the package assembly. Slots in the copper interposer strip and adhesive expose the bond pads for wire bonding. Vias in the polyimide create the solder ball connection points for eventual interconnection from the flex circuit to the PCB.

Assembly manufacturing practice with the enhanced BGA package substrate is more straightforward than that with flex-only substrates, because the metal stiffener is the same material and thickness is used as that incorporated in many leadframe-type packages (e.g., 5-mil-thick leadframes from gull-wing packages). Thus, handling and processing through standard equipment at die attach and wire bond is similar for the enhanced BGA as for quad flat packs and other leadframe-type devices. Likewise, the manufacturing parameters for the downstream assembly processes of overmolding, ball placement, and singulation-sawing is similar for enhanced BGAs as for plastic ball-grid arrays [6].

Board-Level Reliability

Board-level reliability became an important issue as the industry moved from quad flat pack style packages to BGA packages. Both PBGA and cavity-down TBGA packages have since proven their ability to survive most IC environments, however, this can not yet be said for the more recent class of chip scale and near chip scale packages. A major difficulty with these smaller packages is that the substrates are typically much thinner and nearly all the solder joints are directly beneath the die (coefficient of thermal expansion of 3 ppm/°C), thus, if not managed properly, the thermal cycle stress can be quite high. A compounding issue is that these packages have a much finer ball pitch (0.5mm – 0.8mm) than conventional BGAs and thus have a significantly smaller solder joint (ball diameters of 0.3mm – 0.5mm). Higher stress concentrated on a smaller solder joint can be a recipe for failure. To be used in a wide variety of applications these small packages must pass certain minimum standards for board level reliability.

Board level reliability data has been generated for a number of CSP packages in the last couple of years [2,3,7,8,9]. However, it seems there can be a wide discrepancy in the results due to variation of a number of important factors. For example, the board level reliability depends heavily on the coefficient of thermal expansion (CTE) of the test board, the test board thickness, the rate of temperature cycling, the package size, die size, solder ball size/pitch, and elastic modulus of materials, to name a few. It can therefore be quite difficult to compare the results of these separate investigations. In a recent paper by Theo Ejim, he correctly points out that of most importance in these CSP packages (or BGA packages for that matter) is the effective CTE on the ball side of the package under the die [3]. Although board level reliability testing is still necessary to determine the actual reliability of a specific package for a particular application, studying package CTE is a more effective way to quickly compare between package types.

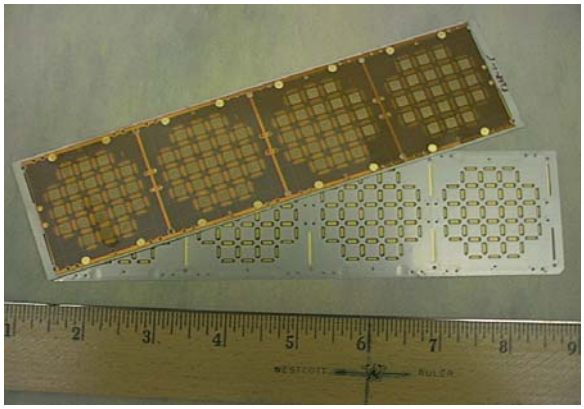


Figure 4. Cavity-Up Enhanced BGA substrate of 7mm (64 I/O) packages at 0.5 mm ball pitch in a 4 an array format yielding 84 packages per substrate.

An effective method of measuring the CTE of a package is to polish off the solder balls and replicate a cross grid pattern of fine lines onto the underside of the package at elevated temperature. A reference grating of 2400 lines/mm is used to generate the moire' pattern at room temperature. The following equation is used to determine the CTE of the package:

$$CTE = \Delta N/(f \times \Delta L \times \Delta T) \times 10^6$$

Where: ΔN is the number of fringes counted
ΔL is the measured length
ΔT is the temperature change
f is the #lines/mm in the grating

Since most circuit boards have a CTE in the range of 15-18 ppm/°C, board level reliability is optimized by designing the package to fall within this range. There have been several methods of influencing package CTE. For instance, the basis behind the Tessera μBGA™ was to control the CTE mismatch by placing a compliant interposer between the die and the solder balls. This 6 mil compliant interposer works

well and results in a calculated effective CTE of 15.7 ppm/°C for a 10mm die [10]. The actual measured CTE of this package (6x8mm in size) using the moire' fringe method described above was 14 ppm/°C [3]. A wire bonded flex BGA package only has a thin die attach adhesive separating the die from the solder joint. In this case the CTE is quite low, measured to be 4.3 ppm/°C under the die [3]. A small PBGA using a thin BT laminate results in a CTE near 9 ppm/°C and this can be modified by changing the BT laminate thickness.

The CTE of the cavity-up enhanced BGA package is controlled by incorporating a metallic interposer between the die and the solder joints. A 125µm thick copper interposer with a CTE of 16.6 ppm/°C appears to be quite effective at shielding the CTE of the die from the solder joints. To prevent stress build up at the die/copper interface, a low modulus die attach adhesive is used. A fully assembled 12 mm, 144 I/O package with an 8.7 mm die resulted in a CTE of 15.5 ppm/°C (moire' fringe pattern shown in Figure 5). Board level reliability results are forthcoming, however, the package is expected to perform quite well.

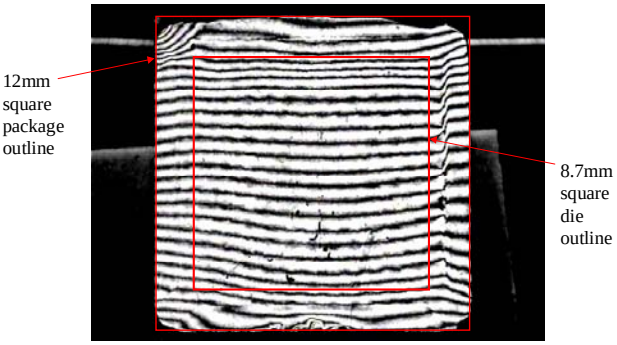


Figure 5: Moiré fringe pattern for the cavity-up enhanced BGA 12mm package. Method reveals a package CTE of 15.5ppm/°C.

The various package CTE values are shown in Table 1 along with some measured thermal cycle results.

Table 1. CTE Values for Various Chip Scale Packages

Package Description	Package & Die Size	Effective CTE (ppm/°C)	0/100°C cycles to 1% failure [3]
Cavity-Up Enhanced BGA (CUE BGA)	12 mm package 8.7 mm die	15.5	
µBGA	5.8 x 7.5 mm	14	>9000
Rigid organic laminate (PBGA)	4 x 6 mm die	9	2900
Ceramic CSP (flip chip)	7 x 7 mm die	7	
Wire bond flex BGA	9 x 6 mm package 4.3 x 6.4 mm die	4.3	500

Package-Level Reliability Testing

Development of a package of a particular size to fit a specific application usually begins with the identification of die attach adhesive and overmold or encapsulant assembly material combination(s) that together with the substrate materials and construction will pass JEDEC A112 Level 3 or 4 moisture resistance testing (MRT) and JEDEC A113 pressure cooker testing (PCT) and thermal shock or cycling. As development proceeds, higher JEDEC levels (1 and 2) are often required and other tests are often performed (e.g., high-temperature storage, dye penetration test).

Whereas ultimately level 3 has often been acceptable in the past (e.g., most PBGA materials made with BT resins perform to Level 3), there has been a recent desire for Level 2, because of the less stringent storage constraints faced by manufacturers/contract assemblers (see Table 2).

Enhanced BGA Package-Level Reliability Studies

Although the polyimide part of the package absorbs moisture up to 2-4%, both flex-only BGA and enhanced BGA packages have proven to be extremely moisture or "popcorn" resistant under PCT and MRT conditions, evidently because the moisture is able to pass out of the package without destroying adhesion at the package interfaces ("popcorn"). For the enhanced BGA, the bare carrier itself (stiffener laminated with adhesive to the flex circuit) has passed JEDEC Level 1 MRT and Pressure Cooker conditions without any voiding observed in CSAM through scans, thus the moisture resistance of the package is controlled by the choice of assembly materials and assembly process conditions.

Table 2. Some Common Package-Level Reliability Specifications and Test Results for 12mm x 12 mm and 7mm x 7 mm Enhanced BGA .

JEDEC Level and/or Test Name	"Out of Bag" Life at 30 °C 85% RH	Test Exposure	12mm Package (d/a #1, o/m #1)	12mm Package (d/a #2, o/m #1)	7mm Package (d/a #3, o/m #2)
Level 1 (JEDEC A112)	Unlimited	168h 85 °C 85% RH	Not tried	Not tried yet	0/10 (Hana)
Level 2 (JEDEC A112)	1 year	168h 85 °C 60% RH	8/8 (fail)	0/8	0/10 (Hana), 0/9
Level 3 (JEDEC A112)	1 week	192h 30 °C 60% RH	0/10, 0/9	0/8	0/10 (Hana), 0/9
Pressure Cooker Test - PCT (JEDEC A113)	-	96h	0/9	Not tried	Not tried
		168h	1/10	0/8	0/22 (Hana)
		240h	Not tried	0/8	0/9
		504h	Not tried	Not tried	0/22 (Hana)
Dye Penetration Test	-	30minutes 65psig	Not tried	Not tried	0/22 (Hana)
Liquid-to-Liquid Thermal Shock	-	500 cycles -65 °C to 150 °C	Not tried	Not tried	0/22 (Hana)
High Temp. Storage – HTS (Mil Std 883D)		1000 h 150 °C	0/7	Not tried yet	0/9 (500h, test still in progress)

Package Codes:
x/y = x parts failed / y parts tested
(Hana) = testing results from Hana Technologies, Ltd., Hong Kong {6}
d/a #1 = die attach adhesive material #1
o/m #2 = overmold material #2

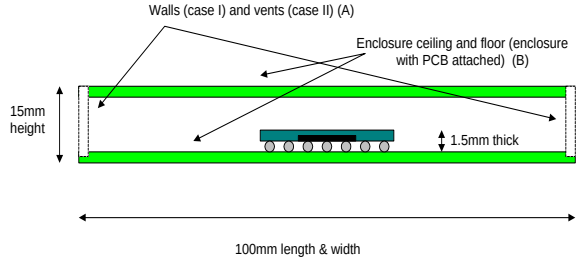
Preliminary screening of the adhesion in moisture environments of a series of die attach adhesives and overmold compounds mounted on top of the same stiffener surface that the enhanced BGA uses, a 100 microinch-thick dull-nickel-plating over copper, was available to select materials for 12 mm x 12 mm enhanced BGA package reliability testing. Materials from the assembly packaging infrastructure were chosen with an emphasis on those used commonly for thin packages and BGAs. The reliability results for these assemblies and 7mm x 7mm assemblies with different assembly materials combinations (see Table 2) show excellent moisture resistance (e.g., passes Level 1 with 7 mm package) and thermal stress resistance (liquid-to-liquid thermal shock and HTS). Some tests have not yet been

completed or are just underway. Air-to-air thermal cycling (not shown in Table 2) is also in progress.

Thermal Design

Greater silicon integration and enhanced device performance has increased the power requirements in many leading-edge, logic devices for portable electronics. Weight and size, particularly thickness, is critical in many of these applications. These physical constraints preclude the use of traditional heat sinks and fans for forced convection cooling. Integration of the copper stiffener in a flex-based BGA substrate is well suited for this new thermal design paradigm. Heat is conducted away from the die along the copper stiffener within the package construction and transferred into the system board through the grid of solder balls. Because the flex circuit is laminated with the traces facing the copper stiffener, the only non-thermally-conductive interface in the package is the polyimide-based thermoplastic adhesive that bonds the flex to the stiffener. The resulting thickness of this adhesive at the solder ball pad locations after lamination is nominally held to 25 microns which minimizes its impact on the thermal path. Since the principle thermal dissipation mechanism is conduction rather than convection in this environment, the relatively low thermal conductivity of the overmold compound is not a factor in the overall thermal performance of the package. This enables the package assembler to utilize the same cavity-up die attach, wirebonding and overmolding assembly techniques that are currently used in high volume PBGA assembly and still produce a thermally enhanced package.

Figure 6. System-level model construction. Refer to Table 1.



Please note that the sketches are drawn to illustrate features of particular importance to the thermal modeling and not all features are drawn to scale.

Tight constraints on the overall form-factor of many high performance portable electronic products has also driven higher wiring density in the system board design and prompted the incorporation of micro-via construction techniques in the system boards for many of these applications. Thinner dielectrics and greater via densities afforded by the micro-via technology can significantly enhance the thermal conductivity of these boards and substantially augment the thermal conduction mechanism employed in the system design. In the end, this becomes a very cost-effective means of thermal management at both the component and system level.

To illustrate the effectiveness of the integral copper stiffener, a 27mm flex-based BGA component was modeled with and without a 125 micron thick copper stiffener in two thermal environments that would typically be encountered in high performance, portable electronics systems. The models were constructed using *Flotherm* v 2.1 [11] and details of the component and system model construction are summarized in the sketches in Figures 6 and 7 and Table 3.

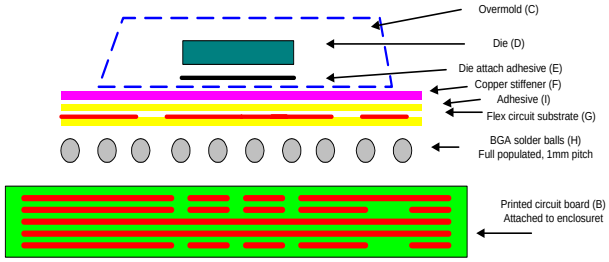


Figure 7. Exploded sketch of component-level model highlighting interfacial materials utilized in the construction. Refer to Table 1. Please note that the sketches are drawn to illustrate features of particular importance to the thermal modeling and not all features are drawn to scale.

Table 3. Summary of key dimensions, material properties, and thermal modeling techniques employed in thermal simulations.

Parameter	Description	FLOTHERM Primitive
System enclosure (A)	100mm x 100mm x 15mm. No radiation to walls and no convective heat transfer from outside walls (in or out). Note: These system-level assumptions are being refined in further work in natural convection cases. Two design cases were considered: (1) vents on two sides allowing 0.5m/s of air flow and (2) all sides enclosed allowing no external air flow.	Walls modeled as thin cuboids with non-radiative interior or exterior surfaces. Ambient temp set at 22.3 C. Horizontal orientation wrt gravity (gravity in –Z direction—worst case for natural convection).
PCB (B)	Printed circuit board with two 1 oz. Power and ground layers and 4 signal layers. Estimated via density of 200 – 300 vias / sq inch. PCB attached directly to outside enclosure.	PCB primitive with no thermal load and 10% copper. (orthotropic conductivity automatically set by software based on copper content and via density).
Overmold (C)	22mmx22mmx1mm (0.5mm above the top of the die). Filled epoxy.	Cuboid with isotropic conductivity K=0.65W/mK.
Die (D)	0.5mm thick 16mm x 16mm Silicon. Die heat source of 5 W used in all runs.	Cuboid with heat source. Temp dep. thermal conductivity 117.5 W/mK @ 100C and linear slope of -0.42 W/mK^2
Die attach adhesive (E)	50 micron thick adhesive with K=1.0W/mK	Cuboid 16mm x 16mm x 0.050mm. K=1.0W/mK.
Stiffener (F)	125 micron thick Cu Alloy 194 (K=262W/mK)	Cuboid with constant K=262. Independent of temperature
Flex (G)	50 micron polyimide with copper traces	Cuboid with smeared conductivity to represent copper ground traces emanating from die pad region. Keff=20 W/mK (5% copper)
Solder balls (H)	1.0mm pitch fully populated solder ball array. Solder balls are asumed to be 0.5mm in diameter.	Collapsed cuboid with orthotropic conductivity of 6.06 W/mK and effective thickness of 0.5mm
Polyimide based adhesive (I)	25 micron thick at solder ball pads (50 microns – 25 microns for copper thickness)	Cuboid 27mm x 27mm x 0.025mm. K-0.20W/mK

Junction temperatures resulting from simulations of each design case are summarized in Table 4. The results indicate that in both system design cases, the device junction temperature was substantially lower in the flex-based package with the copper stiffener. It should be noted that this example case involves a fairly large, 16mm die. The large silicon die helps to spread the heat in the “flex only” construction. This reduces the impact of the copper stiffener on the thermal efficiency of this package. Work is currently underway to

examine the impact of the copper stiffener in applications with smaller die. It is anticipated that the copper stiffener effect will be more profound in these applications.

Table 4. Thermal Simulation Results

System Design Case	Junction Temperature°C) for Flex-Based BGA without Copper Stiffener	Junction Temperature°C) for Flex-Based BGA with Copper Stiffener
No side vents in enclosure	124	103
Side vents allowing 0.5 m/s of air flow	105	85

Electrical Design

In general, flex-based BGA packages offer several electrical design advantages over standard, cavity-up BGA packages based on printed circuit board technology. The most apparent advantage is the high wiring density that can be achieved on a single routing layer. The production design rules for 3M Microflex, for example, currently allow 30 micron lines and spaces in high volume production and 25 micron lines and spaces in small volume runs. This allows substantial design flexibility to include interleaving ground reference traces in the design to minimize simultaneous switching noise and reduce cross talk. More importantly, these design rules allow very tight spacing in the wirebond pad layout area which moves the substrate pads closer to the die pads and reduces the wirebond length. Since a large portion of the total inductance of a BGA package net is a consequence of the wirebond interconnect [12], reducing this length can substantially reduce the total inductance of the package. These advantages are well known and have been previously reported [13].

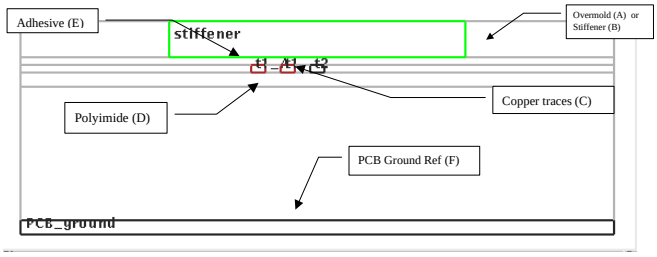


Figure 8. Basic cross section for electromagnetic analysis.

Integration of the copper stiffener into the flex-based BGA construction further enhances the electrical performance by adding a reference plane in the package. The unique construction described earlier puts the signal traces in very close proximity to this reference plane. This effectively reduces the self inductance of the traces which minimizes the simultaneous switching noise in the package. The close proximity of the reference plane also reduces the mutual inductance which minimizes the cross talk in the package.

To illustrate this effect, a 2D cross sectional model of a flex-based BGA package was developed using OptEM, a boundary element electromagnetic wave solver [14]. The basic dimensions and electrical properties used in the model are outlined in Figure 8 and Table 5.

Two signal traces and a ground trace were placed in the cross section to represent typical fanout wiring in the BGA design. In addition, three different constructions of the flex-based BGA were considered in the modeling. In the first case, there was no conductive stiffener in the construction and the traces on the flex were completely encased in the overmold compound. In the second case, a conductive stiffener was placed in the construction as illustrated in the Figure 8, but the stiffener was treated as an additional conductor rather than a ground reference. In both of these cases the ground return current was carried on the PCB ground plane and adjacent ground trace on the wiring layer. In the third case, the stiffener was grounded and carried return current along with the other ground return paths described in the earlier cases.

Table 5. Material Properties used in the Package Construction

Material	Thickness	Conductivity	Dielectric Constant
Epoxy overmold – flex based BGA only (A)	125 µm	NA	Er=3.3, Tanδ=0.026
Stiffener – enhanced flex-based BGA only (B)	125 µm	1.72 µΩ*cm	NA
Copper traces (C)	25 µm	1.72 µΩ*cm	NA
Polyimide (D)	50 µm	NA	Er=3.5, Tanδ=0.010
Polyimide-based adhesive (E)	25 µm (at top of traces)	NA	Er=3.4, Tanδ=0.010
PCB Ground Ref. (F)	25 µm (500 µm separation from package traces)	1.72 µΩ*cm	NA

Although there is a certain amount of commonality in the BGA fanout designs, there is also some room for design flexibility. This is particularly true in flex designs because of the very fine pitch wiring capability. The electrical performance, therefore, can be influenced by the design layout as well as the overall construction. To account for this design dependence, the distance between the signal traces and the corresponding ground trace is called out as a variable in the model as outlined in Figure 9.

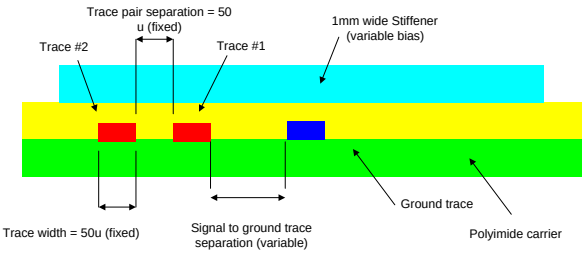


Figure 9. Cross sectional sketch of signal and ground trace positions for each design.

Figures 10 and 11 show the resulting inductance values of the equivalent circuit extractions from the various cases described above. Figure 10 shows the self inductance for trace#1 (refer to Figure 9) as a function of frequency over three decades between 10 MHz and 10 GHz for the different constructions described above. Similarly, Figure 11 shows the mutual inductance values between the two signal traces (refer to Figure 9) in the construction over the same frequency range.

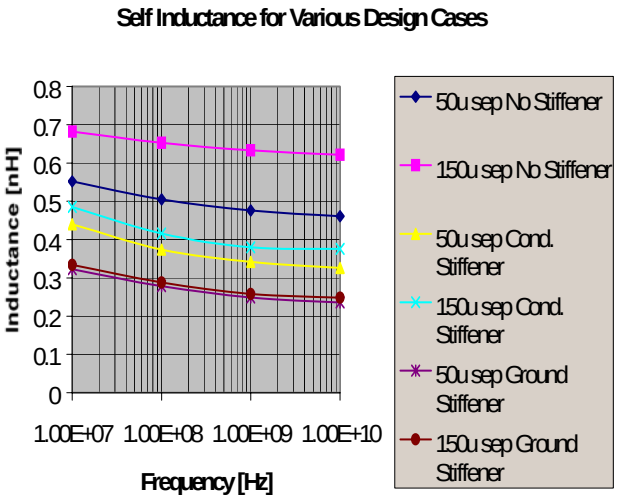
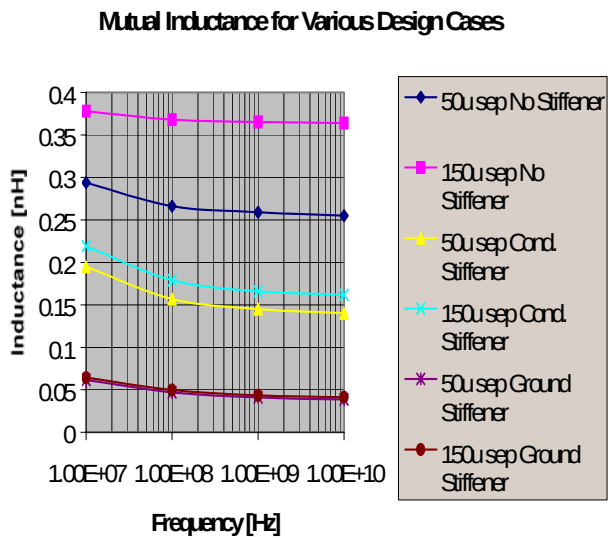


Figure 10. Self inductance values as a function of frequency for each design case.

A close examination of Figure 10 shows the potential impact of the stiffener on the electrical performance of the package. The presence of the conductive stiffener in close proximity to the signal traces reduces considerably the self inductance of the signal traces. This effect is observed even if the stiffener is not specifically grounded due to the generation of displacement currents on the stiffener. When the stiffener is fully grounded, the effect is even more profound because the return current is being carried on the stiffener, thus forming a very tight inductance loop. Further, the presence of the conductive stiffener makes the inductance of the individual traces less dependant on the circuit layout. This can be seen by examining the difference in the self inductance of the trace as a function of the separation distance to the adjacent ground trace for each design case. The flex-based BGA with no conductive stiffener references the ground plane in the PCB which is 0.5mm away. As a result, the individual ground traces on the flex circuit have a more profound influence on the inductance loop. This is reflected in the disparate results shown in Figure 10 for the 50 micron and 150 micron ground trace separations in the "flex only" design case. Actively grounding the stiffener eliminates this disparity between the 50 micron and 150 micron ground trace separations. The conductive stiffener largely compensates for this effect even when it is not actively grounded. The mutual inductance values shown in Figure 11 show a similar pattern and are mainly due to the same electromagnetic effects.



Finally, the values are reported over a wide frequency range in both Figures 10 and 11. This helps to put the observed effects of the stiffener in the context of the expected reduction in self and mutual inductance at increasing frequencies. Please note that the nature of the 2D analysis does not effectively permit us to consider resonance effects. These effects would likely be dependant on the product outline dimensions and individual circuit layouts and, thus, would be design specific.

Figure 11. Mutual inductance values as a function of frequency for each design case.

Conclusions

A new enhanced ball-grid-array (BGA) package with cavity-up orientation and a stiffened flex circuit-leadframe structure has been modeled or demonstrated to have reliability, thermal, and electrical performance advantages as compared with many other prominent flex-only-based and BT-laminate-based (e.g. PBGAs) BGAs and CSPs. These characteristics make this cavity-up enhanced BGA package more suitable for demanding applications where package size reduction is important.

Acknowledgments

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References

1. BPA Group Ltd., "Technology Update No. 3", Feb. 1998, p.2.
2. Newman, K. and Yuan, M., "Board level evaluation of various chip scale packages, *Proc Chip Scale International '98*, May 6, 1998, Santa Clara CA, pp. 99-104.
3. Ejim, T. I., "High reliability telecommunications equipment: a tall order for chip scale packages", *Chip Scale Review*, Vol. 2, No. 5 (1998), pp. 44-48.
4. Prismark Partners LLC, "Chip Size Packages – We Have Lift Off", December, 1997, pp 2-10.
5. Schueller, R. D, Bradley, E. A., Harvey, P. M.., "Flex Based Chip Scale Packages – Meeting the Cost/Performance Challenges", *Chip Scale Review*, January-February (1998), in press.
6. Hayden, T. F., Clatanoff, W. J., del Rosario, E.. and Opiniano, E., "Assembly and Package Reliability of a New Flex-Based Fine Pitch BGA", submitted for *IPC Chip Scale and BGA National Symposium*, Santa Clara, California, May 1999.
7. Darveaux, R., Heckman, J., and Mawer, A., "Effect of test board design on the 2nd Level Reliability of a fine

pitch BGA package", *Proc Surface Mount International*, San Jose, California, Sept. 1998, pp.105-111.

8. Uegaki, S., "Ceramic CSP – current status of technology", *Proc Surface Mount International*, San Jose, California, Sept. 1998, pp.179-188.
9. Bauer, R., "Advances in chip scale packaging", *Proc Surface Mount International*, San Jose, California, Sept. 1998, pp.173-177.
10. Clech, J. P., "Flip-chip and chip-scale package reliability modeling", *Chip Scale Review*, Vol. 2, No. 5 (1998), pp. 49-54.
11. *FLOTHERM* is a computational fluid dynamics analysis tool that has been tailored specifically for the electronics industry. It was developed by Flomerics Limited, Hampton Court, Surrey, UK.
12. Lau, J., Ball Grid Array Technology, McGraw Hill (New York, 1995), pp. 346-348.
13. Harvey, P., Schueller, R.D., and Kinningham A., "Cost-Effective TBGA Design and Construction for High Reliability and Enhanced Electrical Performance" *Proc Semicon Taiwan*, Taipei, Taiwan, Sept. 1997, pp. 85 – 95.
14. OptEM package analysis tools, OptEM Engineering Incorporated, Calgary, Canada.