Flex Based Chip Scale Packages – Meeting the Cost/Performance Challenges

R. D. Schueller, E. A. Bradley, and P. M. Harvey
3M Electronic Product Division
Austin, Texas

Introduction

A number of terms have been used to refer to small form factor packages, such as chip scale, chip size, near chip scale, and fine pitch. However, the name is not as important as the user's concerns that the package is small enough for the application, the reliability and performance is sufficient, and the total applied cost is minimized. The term chip scale package (CSP) will be used for this paper. The authors believe this widely-recognized term best describes the variety of small form factor packages that are becoming increasingly popular among designers of portable electronic devices, laptop computers, telecommunication systems, and other areas where size is of critical importance. The authors recognize, however, that not all formats of the packages discussed in this paper are technically CSPs (<120% of the chip size).

Because of the demand for CSPs and the large number of creative individuals in the field, there is no shortage of package options. The over 50 available CSPs are often grouped in four categories according to their substrate:

- lead frame based
- rigid substrate based (PC board or ceramic)
- wafer level
- flex circuit based

Flex is the market leading CSP substrate and is the focus of this paper. According to TechSearch International, there will be 861 million flex circuit based CSPs sold in the year 2000, which is nearly half the overall CSP forecast of 1885 million units [1]. A BPA report predicts flex substrates will be used for 57% of CSPs in the year 2002 [2].

Flex circuits have an attractive combination of characteristics suited for this market. A number of flex producers today can handle design rules of less than 65 μm pitch, whereas circuit boards are closer to three times this value. Consequently, most of the fine pitch BGA patterns (as low as 0.5 mm ball pitch) can be routed on a single metal layer. The via sizes on traditional PCBs (typically 0.5mm or larger) can make routing these finer ball pitch packages all but impossible [3]. Flex circuitry is also not new to the packaging industry. In the form of TAB tape, flex has proven itself to survive the harsh reliability conditions expected of an IC package. PC boards, on the other hand, are relatively new as a first level interconnect substrate, with BT resin having been the first to prove itself capable. Another important advantage of flex is that there are numerous producers in the market, providing for a more stable source of supply. Users are sensitive to this fact due to issues experienced with a sole source of supply for BT resin. Flex also provides a thinner package, which can be advantageous in a number of applications.

There are a large number of flex based CSPs available. However, only a few of the more prominent ones will be mentioned in this paper, examining advantages and appropriate market segments.

Wire Bond Flex BGA

Today, wire bond flex BGA (known as μStar™ at TI and *fle*XBGA™ at Amkor) is the highest volume form of flex based CSP. This construction is illustrated in Figure 1. There are many companies developing this type of package, and according to Prismark it makes up 60% of the world's currently shipped CSPs [4]. The main advantage of this package is its simplicity and low potential cost. The assembly of the package follows closely the standard PBGA packaging process, with the only modification being an added

procedure for rigidizing the flex so it handles like a strip. There are two main methods of achieving this goal; one is to align the tape to a metal fixture with tooling pins, and another is to laminate a metal frame using an adhesive.

This appears to be the lowest cost packaging method since for most die sizes, the package can be routed with low cost, single metal layer flex. For example, a ball array 4-6 rows deep can be routed at 0.8 mm pitch. Since this package can easily support either a fan-in or fan-out ball array (or combination thereof), a larger number of balls can be routed by slightly expanding the package body size. This versatility also enables the package to be designed to minimize expensive fine pitch routing on the board. In addition, the die size can shrink while still using the same package and footprint.

There has been some concern about board level reliability of this type of package due to the close proximity of the die to the board with only the die attach adhesive providing compliance for CTE mismatch. However, data generated by Amkor and Motorola (Figure 2) has shown that this package with 0.8 mm ball pitch and die sizes of less than 10 mm provides sufficient board level reliability for many applications [5].

Some potential shortcomings of this package include:

- Extra handling required for flex
- Board level reliability for 0.5 mm ball pitch and for larger die/package sizes
- Requirement for a solder mask dam to prevent adhesive bleed onto wire bond fingers

μBGA™

The Tessera μBGA package is arguably the best known of the flex based CSPs. Figure 3 shows its construction. Modifications such as gold plated copper leads and silicone nubbins have been made over the years to improve this package, however, the concept is basically unchanged. A compliant elastomer layer is used to isolate the CTE mismatch stress of the die from the motherboard, prolonging the solder joint life. The μBGA has also proven itself to be quite moisture resistant, and is qualified to JEDEC level 2 [6]. In its standard form, this is a true chip size package, therefore it only enables a fan-in ball layout. This makes it a good solution for applications with a high die size-to-ball count ratio (such as various memory die), but it is less attractive for applications where some degree of fan-out is desired. Incompatibility with existing infrastructure is the largest barrier to overcome with μBGA, however, much work has been done to develop new process steps and specialized equipment. A thermocompression bond is used to interconnect a lead on the tape to the die, so the versatility of a standard wire bond is not realized but the electrical inductance is minimized. Today, there are a number of licensed assemblers with the ability to manufacture this package.

Enhanced CSP

The E-CSP substrate from 3M is one of the newer constructions in the market. This patent pending product is similar to the flex BGA but includes some significant enhancements. The E-CSP is constructed by laminating a patterned 5 mil copper lead frame to the flex circuit (the carrier strip is shown in Figure 4 and a drawing shown in Figure 5). Typical die attach adhesives are used to adhere the IC to the surface of the lead frame. The IC is then wire bonded to the circuit through slots or openings in the lead frame. Overmolding takes place and the parts singulated from the strip (a cross section is shown in Figure 6). This package provides the following enhancements:

- Improved board level reliability
- Improved heat dissipation
- Easier handling in assembly
- Improved coplanarity for larger packages
- Elimination of solder mask dam

Board Level Reliability

For relatively small die sizes at 0.8 mm ball pitch adequate board level reliability has been demonstrated for many applications with the wire bond flex BGA package. However, as the die grows larger and/or the

ball pitch is reduced, the lack of an adequate interposer will likely become more of an issue. The E-CSP uses the 5 mil copper as an interposer. By using a high temper copper alloy with a CTE value matching closely with that of the board, the solder joint stress normally associated with the low CTE of the die is shielded. A Moire' fringe analysis was performed on the ball side of a fully assembled 12 mm E-CSP package with an 8.8 mm die to determine the effective package CTE in both the x and y direction (shown in Figure 7). A 2400 lines/mm grating was created on the ball side of the package and the CTE measured between a temperature range of 22°C and 82°C. Three samples were measured in both the x and y direction. The resulting mean of 15.5 ppm/°C more closely matches the CTE of a circuit board (typically between 15 and 18 ppm/°C) than would a package without the interposer.

In addition, an Ansys two dimensional mechanical stress/strain model was created to directly compare a 12 mm flex BGA structure to the E-CSP in a board level condition. The model in Figure 8 predicted the Von Mises cumulative effective plastic strain in the solder ball after 5 cycles from –55/125°C. The strain is 88% in the flex BGA compared to only 17% in the E-CSP. The material set selected for this package will determine the package level reliability. Only a few materials have been evaluated thus far. When constructed with JMI2500B or Hysol KO120 die attach adhesive and Sumitomo 6600CR overmold compound, the package passed JEDEC A112 moisture level 3 and 168 hours of pressure cooker testing with no electrical failures. Additional materials are currently being evaluated.

Thermal Enhancement

To determine the heat dissipation capability of the E-CSP package structure, a number of thermal models have been created for packages and die of various sizes. The basic finding is that the copper interposer provides an increasing benefit over a wire bond flex BGA package as the body size-to-die size ratio increases. The copper interposer effectively spreads the heat from the die over all the balls in the package and provides an efficient thermal path to the mother board (Figure 9). The graph in Figure 10 shows comparative thermal results for a 16mm die in a 27 mm package (676 I/O). The 27% difference in Theta J_a between these two structures would increase further as the die size was reduced or if the heat spreader thickness was increased. It is anticipated that the E-CSP structure could handle a die of over 5 watts with no airflow (depending on the specifics of the application of course).

Infrastructure Fit

Handling bare flex has been an important issue since its inception. However, laminating the flex to a rigid lead frame eliminates these issues. Throughout assembly the resulting strip can be handled like a conventional printed circuit board. As with a PCB, the utilized area is a large component of cost with a flex circuit. Minimum cost is thereby achieved though optimization of component density in the strip. For smaller package sizes this often means the packages should be laid out in an array format in the strip and singulated with a dicing saw. The rigid strip format is also more conducive to efficiently performing testing of all packages while still in the strip prior to singulation.

For larger body size packages, maintaining coplanarity of a wire bond flex BGA becomes more challenging since the overmold compound begins to dominate the structure. The authors anticipate that the E-CSP constructed with a 5 or 10 mil stiffener would do a better job of combating the overmold warpage stress. Data on coplanarity for 77 assembled 12 mm packages revealed a mean coplanarity of 1.436 mils with a standard deviation of 0.033 mils [7]. However, data on larger packages needs to be gathered to determine the functional limits.

Flip Chip CSP

Flip chip interconnection has traditionally been used primarilty in two markets. It has been used for direct attachment to a board for low end applications such as watches or for attachment to a multilayer ceramic (or more recently PCB) package substrate for high end mainframe applications. The real volume opportunities, however, lie in the more mainstream midrange markets such as cell phones and personal computers. To penetrate these markets, packaging costs must be brought down to where they are competitive with existing wire bond packages such as QFPs and BGAs (0.6 – 0.8 cent/lead). Direct chip attach to a circuit board is not desired in these markets due to the issues associated with underfill (this process does not fit typical board assembly shop capabilities and rework is very difficult).

A number of companies are currently examining the use of low cost PCB or flex circuit substrates as a flip chip interposer. The chip can be attached and underfilled, the solder balls attached, the package electrically tested, then singulated and presented to the board assembler like any other BGA package. Flex works well as a flip chip interposer due to its finer pitch capability. 2 metal layer flex might be required if the interposer is to be used as a redistribution layer, depending on the ball pitch and I/O count (drawing shown in Figure 11).

There are a number of advantages to flip chip as compared to wire bonding. For example, electrical performance is significantly improved. However, the real driver for mainstream markets will be cost. The process of bumping a wafer, reflow attaching to a substrate and underfilling must be lower cost than die attach, wire bonding, and overmolding. Flip chip has the added advantage of enabling more I/O per unit area on the chip thereby enabling die shrink cost reductions for pad limited die. The graph in Figure 12 shows that for typical ball pitches of 250 μm, a die of over 200 I/O can be reduced beyond pad limited size (assuming 70 μm effective wire bond pitch). If the flip chip ball pitch is reduced further, then pad limited die of even lower I/O count can be shrunk. This calculation does not take into account the size added to the chip to make room for the wire bond pads. A flip chip die has a further advantage since bumps can be placed directly over active areas, thus saving real estate.

A recent paper by Mistry et. al. compared flip chip attach to circuit board substrates of various thicknesses to that of a thin flexible circuit [8]. Surprisingly, it was found that the thin flex actually performed significantly better in board level thermal cycle testing than did the thicker PCB substrates. Thermal cycling from 0 to 100°C resulted in a characteristic life of 5524 cycles with a beta slope of 11.1. This is over two times better than a 1 mm thick PCB substrate.

Although much of the attention in the US has been on solder attached flip chip, it appears that many in Japan are more focused on anisotropic conductive adhesive as an interconnect method. Use of such an adhesive is attractive since it eliminates the underfill process. Due to concerns over reliability, these materials are first being implemented on lower end products with the potential to migrate to more sophisticated applications if the reliability is proven. As more companies begin to seriously focus on implementing various forms of flip chip attach, flex circuitry will likely begin to play an increasingly important role.

Applications for Flex Based CSPs

Flex based BGA packages offer a much needed small form factor package to a variety of markets. Memory is a logical area for flex based packages and the industry has seen successful implementation of both μBGA™ packages as well as wire bond flex BGAs. But because flex substrates offer superior routing capability to rigid substrates they are also ideal for logic devices with higher I/Os. Below is a discussion of the role of flex based CSPs for logic devices in the telecommunications equipment, graphics chip, and portable electronics markets.

Telecommunications Equipment Market

Chip scale package designers have largely overlooked the telecommunications equipment market because one does not typically associate large pieces of equipment with a need for a small form factor package. But this industry can gain large cost savings and increased product functionality by using near chip scale packages. CSPs allow designers to pack more chips and more functionality into a given board size. Therefore, designers can either increase the functionality of the product or decrease the number of boards and lower the overall cost.

The wire bond flex BGA and the E-CSP discussed above are excellent candidates for this market. The combination of the cavity up construction, which allows routing directly under the die, and the fine pitch capability of flex, allow designers to route more I/O in a given area. This is important for telecommunications logic ICs such as ASICs, PLDs, and DSPs that can typically have from 200-500 I/O. In addition to high density routing needs, two other factors play a role in determining what kind of flex based BGA package is used in this market. These include heat dissipation and board level reliability requirements.

A wire bond flex BGAs should be adequate when devices are dissipating less than two watts heat. In many cases, the device is dissipating greater than two watts, so a heat sink must be added or an enhanced BGA is required. As mentioned earlier, the copper interposer in the E-CSP can accommodate heat dissipation by spreading the heat from the die over the balls in the package to the printed circuit board. The exact heat dissipation capability of this package is dependent on many factors including die size, package size, air-flow, proximity to other devices, and the construction of the printed circuit board. Thermal modeling of the E-CSP (Figure 10) provides a theta Ja of less than 16 C/W for a five watt device.

Regarding board level reliability, various factors including die size and ball pitch affect the performance of a package. For the higher performance telecommunications market, die size causes the greatest concern since die can be quite large (over 12 x 12 mm). The copper interposer in the E-CSP de-couples the die from the solder balls, reducing the effect of the CTE mismatch between the die and the printed circuit board.

Graphics Chip Market
Graphics chips for desktop and portable computers have traditionally used cavity up PBGAs. Heat dissipation is important to this market since many devices require 2-10 watts of power dissipation. A PBGA typically requires a heat sink for these applications. The E-CSP package offers improved heat dissipation without a heat sink since it can dissipate up to 50% more heat than a typical PBGA. This allows the designer to exclude the heat sink for devices dissipating less than 6 watts. Eliminating the heat sink lowers the overall cost and reduces the space needed for the package.

In addition to decreasing the height of the package, E-CSP can also provide the same I/O capability in a smaller outline package. For example, 256 I/O can be easily routed on one metal layer flex in a 17mm package, or up to 484 I/O in a 23mm package with 1.0 mm ball pitch. This smaller package can result in a significant cost savings, especially if the E-CSP is used to replace a larger cavity down enhanced BGA.

Portable Electronics Market
The use of CSPs in portable electronics has been increasing rapidly over the last few years. Wire bond flex BGAs are proving their capability by meeting board level reliability requirements, decreasing the area required on the board, as well as providing a thinner package.

The E-CSP offers advantages that may be needed in the future of the portable electronics market. Regarding board level reliability, ball pitch is more of an issue than die size because die sizes are relatively small. As ball pitches migrate to 0.5mm, adequate board level reliability becomes questionable with a flex only package since the opportunity for solder ball cracking will increase with the smaller diameter balls. In addition to the benefit of improved board level reliability, the stiffener also acts as an inhibitor for die attach bleed, eliminating the need for a solder mask or covercoat.

Flip chip CSPs also have an opportunity to play a role in portable electronics as well since form factor is one of the main drivers for this market. As mentioned earlier, however, overall cost must be competitive with wire bond solutions. A simple low cost one metal layer flex substrate should be adequate to route the I/O for many of these applications, but the infrastructure and assembly processes are still being developed for this market.

Conclusions

Flex is the leading substrate for building a chip scale package due to its high circuit density-to-cost ratio. It is also helpful that there are many flex circuit suppliers already in the market. Flex based CSPs with different characteristics are rapidly being developed to satisfy the needs of several market segments. The μBGA™ and the wire bond flex BGA appear to be the leading candidates for the memory market. The needs of the portable electronic market seem to be filled by the wire bond flex BGA today and possibly a flip chip CSP in the future. However, for higher end applications such as graphics and telecommunications the E-CSP may be the best choice due to its improved board level reliability and ability to dissipate heat. Applications which use a peripheral routed enhanced cavity down package today, may turn to a fully populated E-CSP in the future to reduce the package size and cost while maintaining the thermal and reliability requirements.

Acknowledgements

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Authors

Dr. Randy D. Schueller is a Senior Product Development Specialist and DevelopmentTeam Leader for 3M's™ Microflex Advanced IC Packaging Group based in Austin, Texas. He has authored 16 papers and has 4 issued patents in the field of IC packaging. Randy received his B.S. degree in Physics from St. John's University and his M.S. and Ph.D. in Materials Science and Engineering from the University of Virginia. Randy can be reached at (512) 984-5145 or by e-mail at rdschueller@mmm.com.

Elizabeth Bradley has several years experience with 3M Company in business development for the Electronic Products Division. In her role as Market Development Supervisor she is responsible for commercializing technologies, such as 3M™ Microflex, for the IC packaging industry. Elizabeth has a Masters Degree in Business Administration (MBA) from the University of Texas at Austin, and a Bachelor of Science Degree in Mechanical Engineering from Texas A&M University. She can be reached at (512) 984-6699 or by e-mail at ebradley@mmm.com.

Paul Harvey is a Senior Product Development Specialist in the Electronic Products Division Lab at 3M in Austin, Texas. He is a member of the team that is responsible for development of innovative new electronic components and IC packages based on 3M™ Microflex circuit technology.His 15 year career includes technical and engineering assignments in all aspects of research, development, and manufacturing of electronic packaging products. His current research interests include electrical and thermal design and performance analysis and he has published numerous papers on this and other topics related to electronic packaging. He holds a BSChE from Brigham Young University and an MSEE from Syracuse University. He is a member of IEEE and IMAPS. Paul can be reached at (512) 984-5784 or by e-mail at pmharvey@mmm.com.

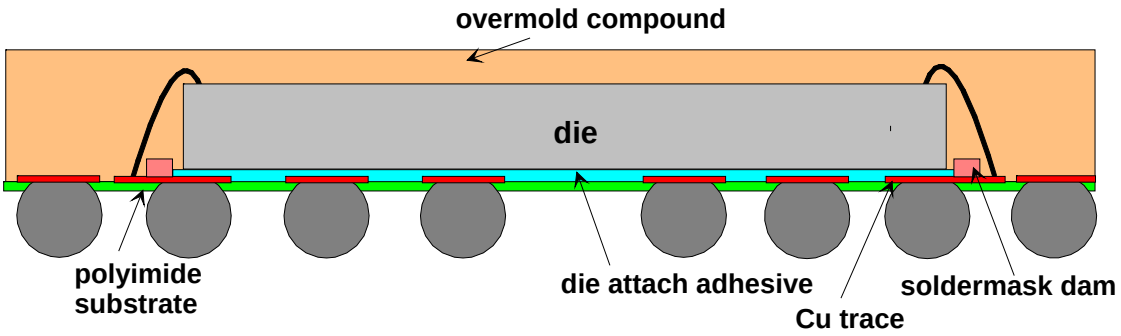

Figure 1. Wire bond flex BGA in a near CSP format (fan in and fan out).

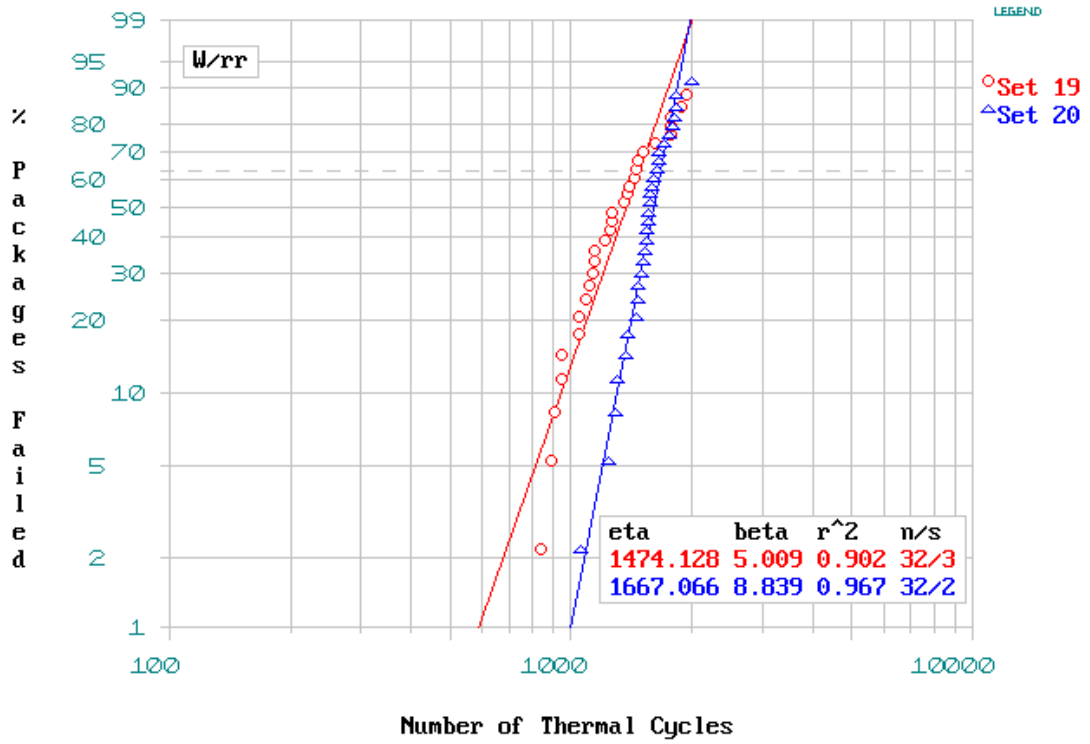

Figure 2. Board level thermal cycle reliability for a 12mm, 144 I/O package with 9.5mm die size (-40C ⇔ 125C, 1cycle/hr). Results are for a 0.9mm thick test board (#20) and a 1.6mm thick test board (#19) [5].

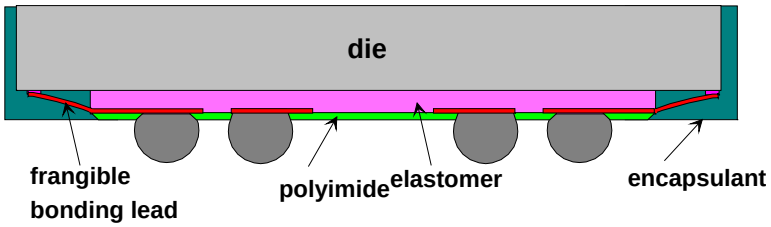

Figure 3. Tessera µBGA™ with fan in ball pattern. Elastomer layer is used to absorb the CTE mismatch strain.

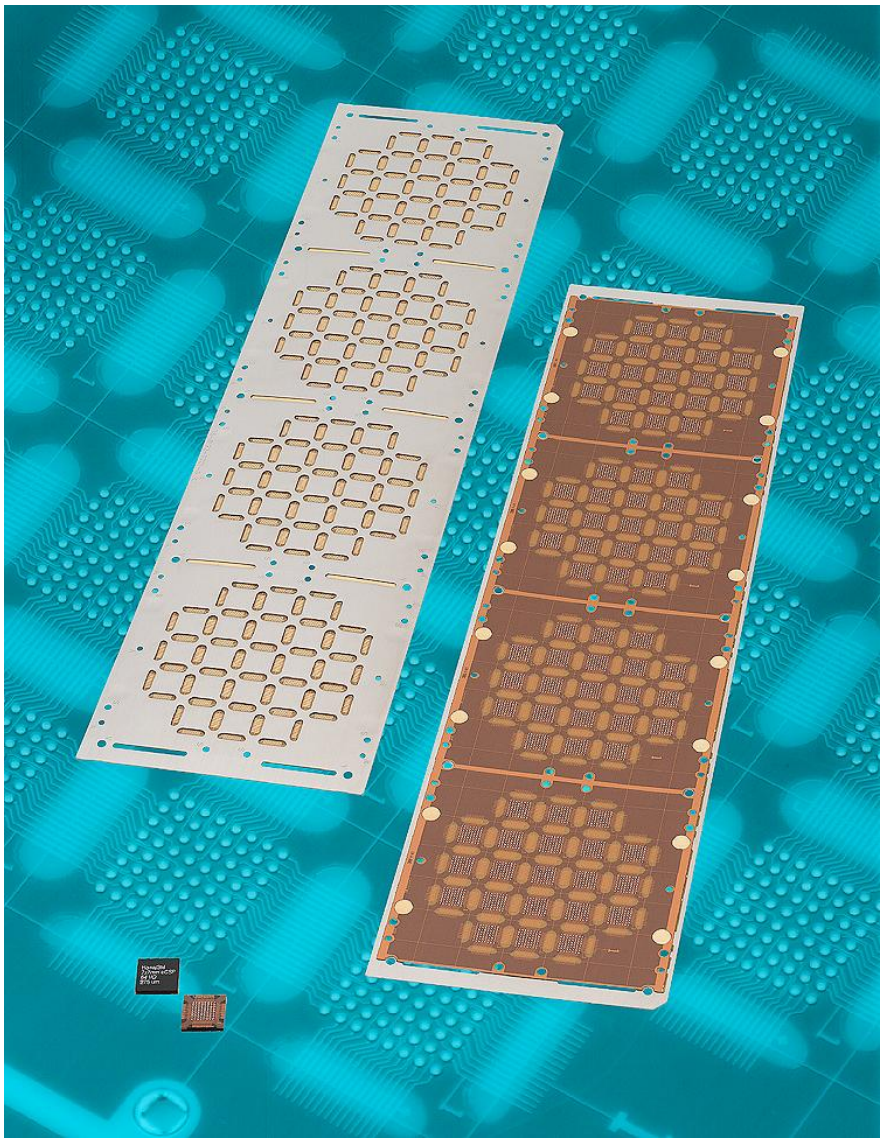

Figure 4. E-CSP strip of 7 mm (64 I/O) packages at 0.5mm ball pitch in an array format.

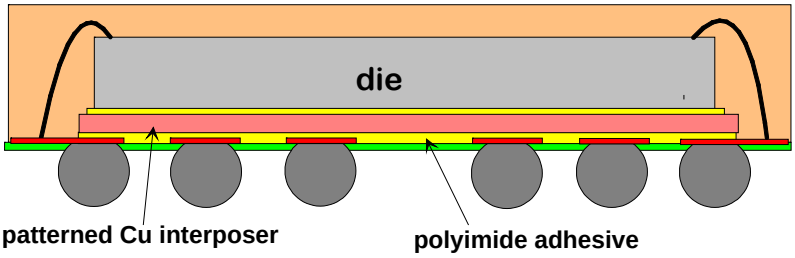

Figure 5. Enhanced CSP structure in a CSP format. Copper interposer enables a matched CTE to the board.

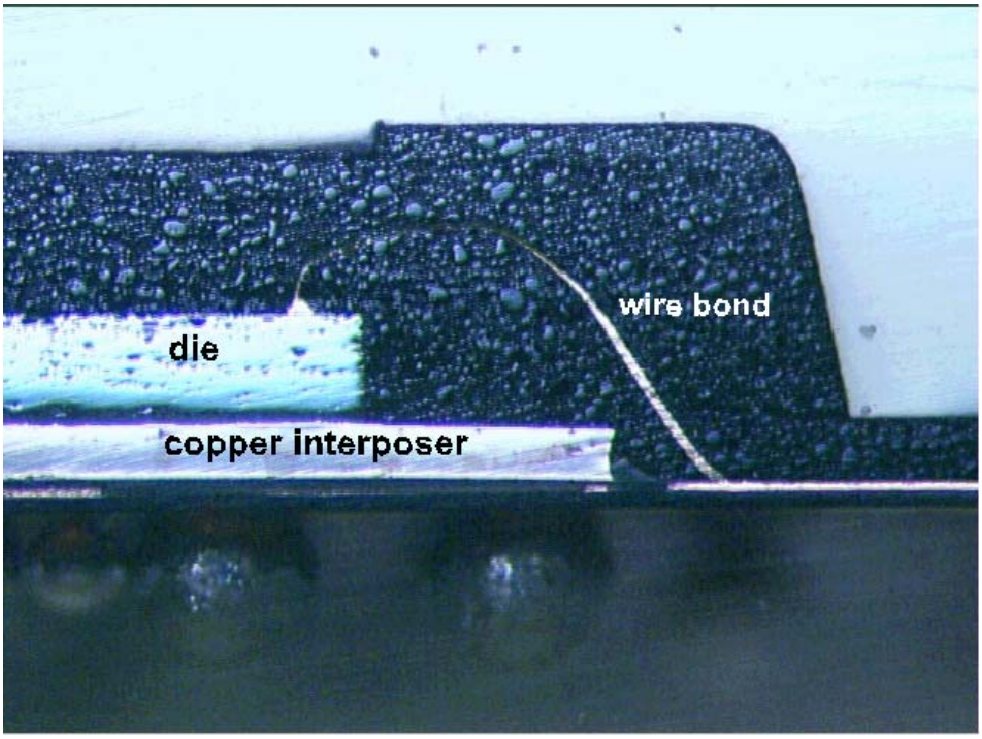

Figure 6. Cross section of an assembled E-CSP (12mm, 144I/O).

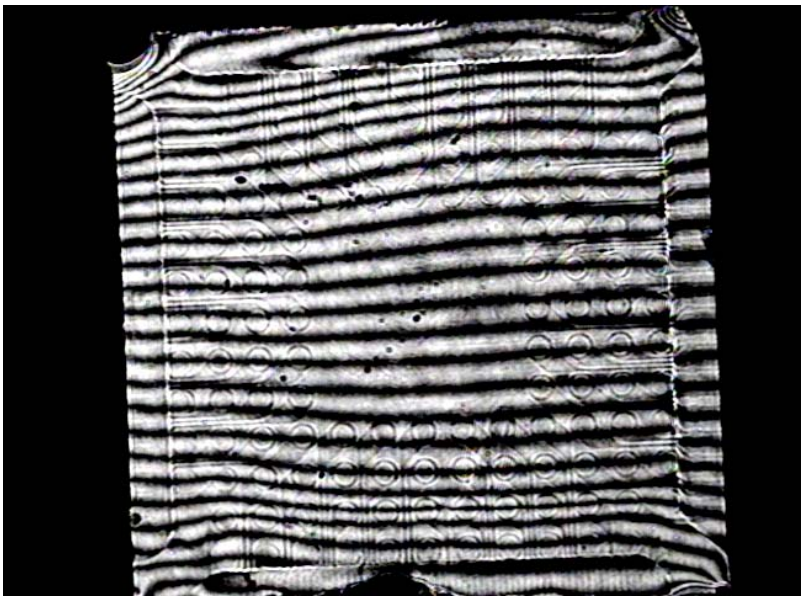

Figure 7. Moire' fringe pattern of an assembled 12 mm E-CSP. Method revealed a package CTE of 15.5 ppm/°C in the x-y direction

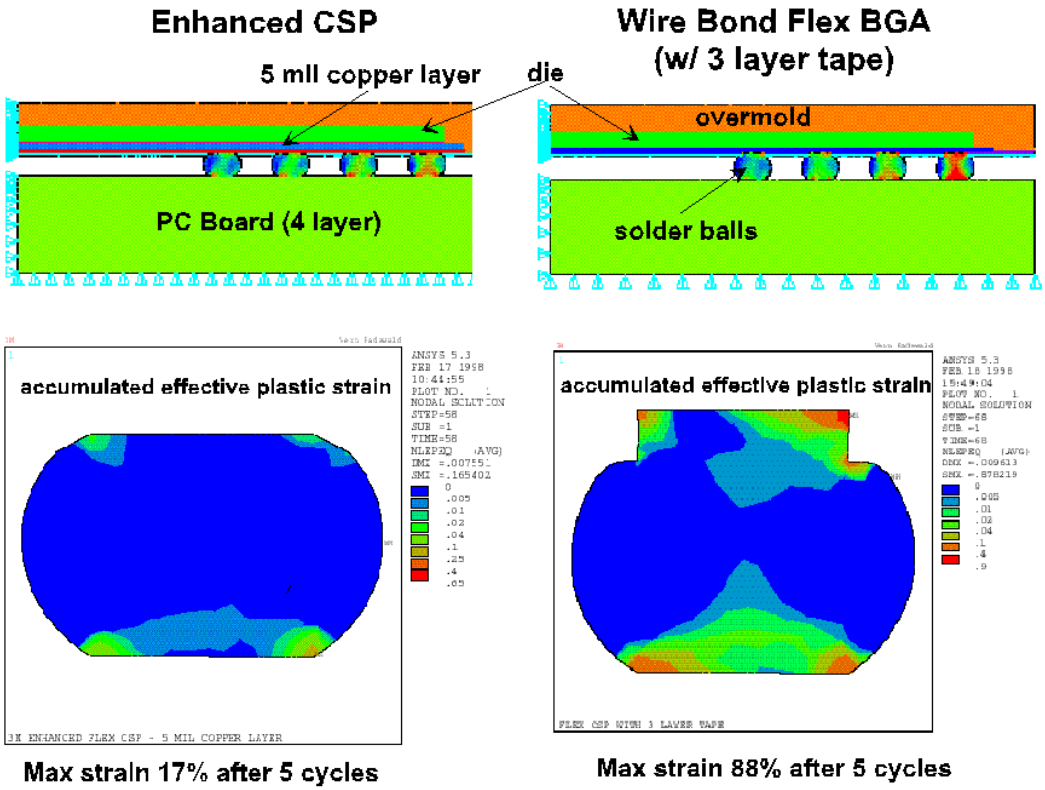

Figure 8. Ansys mechanical stress-strain model for E-CSP compared to wire bond flex BGA when thermal cycled from –55 to 125°C.

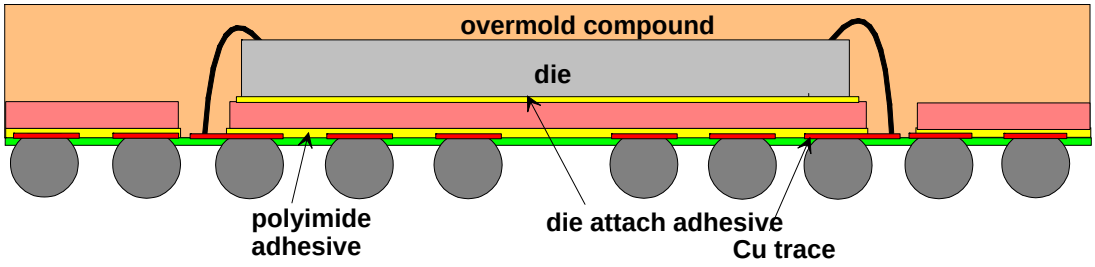

Figure 9. E-CSP structure in a larger format for improved heat dissipation and higher I/O. Slots for wire bond pads are separated by metal tabs at the corners of the package.

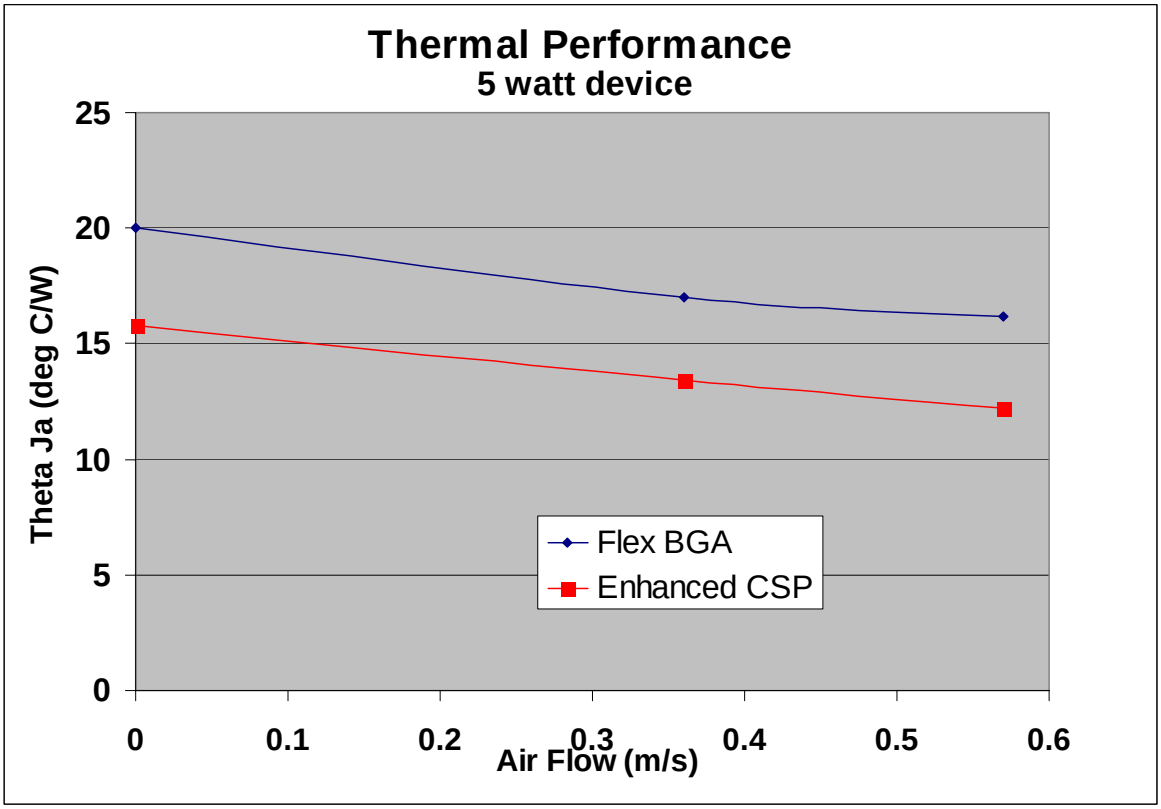

Figure 10. Thermal modeling results for E-CSP compared to a standard wire bond flex BGA. 16mm die in a 27 mm package on a 4 layer PCB.

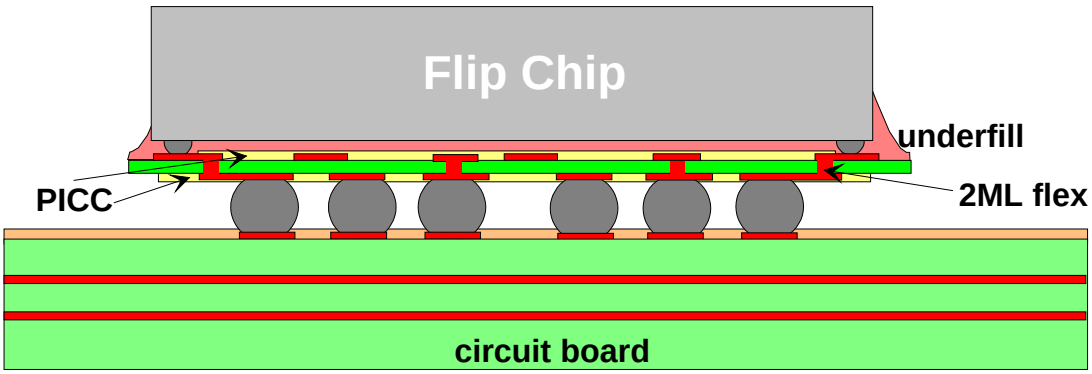

Figure 11. One example of a two metal layer flip chip CSP in which redistribution is performed on the package.

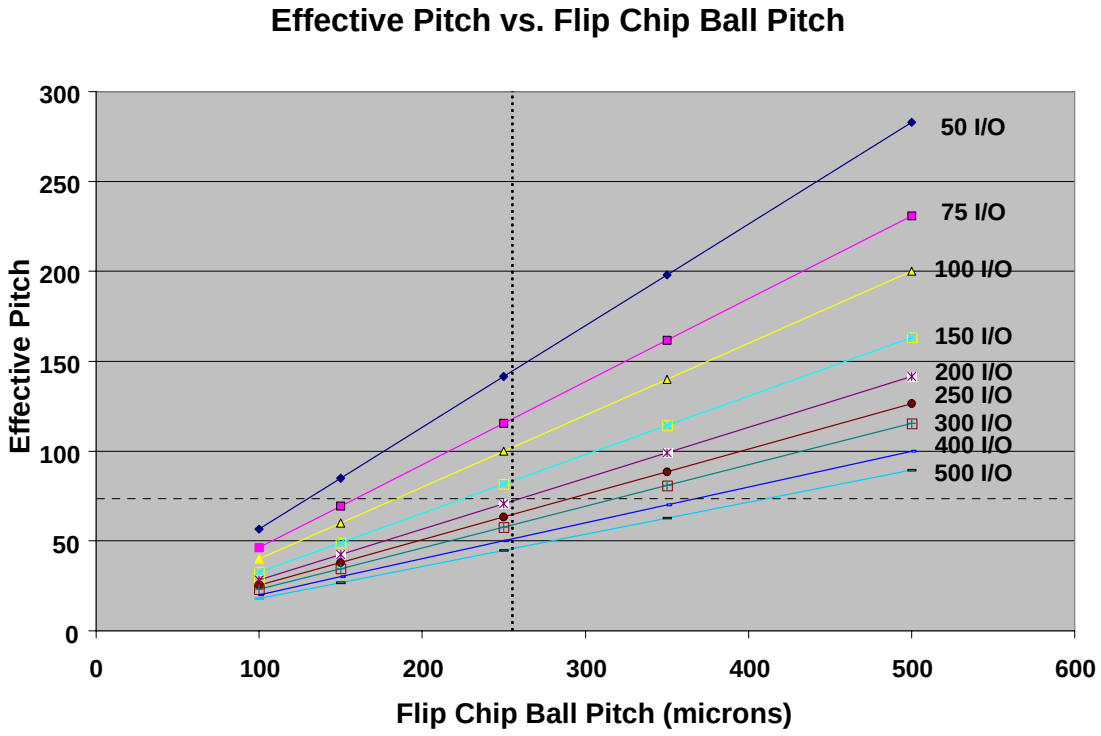

Figure 12. Graph of effective wire bond pitch vs. flip chip ball pitch for various die I/O counts. Situations with an effective wire bond pitch less than about 70 μm enable die shrink.