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Moving Automotive Electronics from Reliability/Durability Testing to Virtual Validation Modeling Using a Physics of Failure CAE App

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ABSTRACT

Quality, Reliability, Durability (QRD) and Safety of vehicular Electrical/Electronics (E/E) systems traditionally have resulted from arduous rounds of Design-Built-Test-Fix (DBTF) Reliability and Durability Growth Testing. Such tests have historically required 12-16 or more weeks of Accelerated Life Testing (ALT), for each round of validation in a new product development program. Challenges have arisen from:

- The increasing number of E/E modules in today's vehicle places a high burden on supplier's test labs and budgets.
- The large size and mass of electric vehicle power modules results in a lower test acceleration factors which can extend each round of ALT to 5-6 months.
- Durability failures tend to occur late in life testing, resulting in the need to: perform a root cause investigation, fix the problem, build new prototype parts and then repeat the test to verify problem resolutions, which severely stress program budgets and schedules.

To resolve these challenges, automakers and E/E suppliers are moving to Physics of Failure (PoF) based durability simulations and reliability assessment solutions performed in a Computer Aided Engineering (CAE) Environment. When PoF knowledge is converted into math models and integrated into CAE durability simulations and reliability assessments tools, it can be determined if and when a device will be susceptible to failure mechanisms over its life cycle.

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INTRODUCTION

Physics of Failure CAE modeling combines dynamic stress analysis of usage and environmental conditions with failure mechanism models to perform a durability simulation on a virtual model of an electronic module in order to identify failure susceptibilities and calculate reliability behavior over time. Finding problems on the CAE screen allows corrective actions to be implemented quickly at low cost without impacting program schedules or budgets.

PoF/RP analysis was first performed using traditional numerical CAE tools such as Finite Element Analysis (FEA). This approach, known as stress-to-strength interference analysis, has long been used in mechanical, structural, construction, and civil engineering. The use of PoF modeling enables a physics based view of product reliability and durability that identifies optimization opportunities early in the design cycle. This approach provides greater insight for creating highly reliable, robust products faster and at lower cost.

The large amount of time and high level of expertise needed to create FEA models for automotive electronic modules has limited their use [1]. CAE Apps have now been developed that automate PoF analysis tasks that allow non-CAE experts to perform expert level evaluations. This paper introduces and provides examples of a PoF CAEs App analysis tool suite for Electrical and Electronic (EE) equipment. The functions of the Sherlock ADATM (Automated Design Analysis), a powerful PoF CAE App tool suite that automates durability simulation and reliability assessment, will be reviewed and demonstrated.

PHYSICS OF FAILURE / RELIABILITY PHYSICS BASICS

PHYSICS of FAILURE (PoF) is a formalized, enhanced form of failure analysis, often performed in a research format. The objective is to identify the ultimate root cause mechanisms, processes, triggers and propagation factors that result in failure of materials, components and systems [2].

RELIABILITY PHYSICS (RP) is the science-based application of PoF research into engineering and product development procedures and tools for producing failure free products and achieving comprehensive product integrity. RP is most effectively used as part of a “Design for Reliability” effort where knowledge of potential failure mechanisms guides designers to avoid problems and optimize a design to produce robust, highly reliable and durable products [3].

PoF/RP modeling integrates reliability into the design activity via a science-based process for evaluating the ability of materials, structures, and technologies to endure stress. The primary issues evaluated in PoF modeling are overstress and wearout-related failures.

- OVERSTRESS FAILURES such as electrical overstress, fractures, yield and buckling occur when the stresses of the application exceed the strength of a device's materials. Overstress causes imminent failures. Items that are well designed for the loads of their application, rarely experience overstress failures. They occur only under conditions that are beyond a device's design intent (i.e. acts of god or war); such as being involved in a crash, struck by lightning or submerged in a flood. Load-stress analysis determines if the strength limits of a design and its components are adequate for the application. Understanding the overstress yield limits of a design is essential for determining if the design is suitable for its application.
- WEAROUT FAILURES are related to gradual stress driven damage accumulation of materials over time (also known as Stress Aging). This covers failure mechanisms such as fatigue, delamination and thermal degradation, along with corrosion and oxidation. PoF analysis for wear out failures involves performing a durability simulation that produces a detailed reliability verses time plot. The basic concepts in Stress-Strength analysis are:
  - LOAD - the amplitude of a condition that causes a change(s) in material properties of the structure or components which the load acts upon [4].
  - STRESS - the average per unit area internal forces inflicted on a material or structure due to load [5].
  - STRAIN - the measure of the change that occurs to a material under stress [5].

In mechanical, civil and structural engineering, CAE structural stress analysis for optimizing performance, durability and reliability requirements is a standard part of the engineering process, that helps to design products and parts right on the first attempt. CAE analysis tools also accelerate and improve the engineering process while reducing the need for physical prototype and durability testing which reduces product development time and costs [6].

By contrast, E/E engineers primarily use CAE tools for circuit, functional and software analysis. E/E Engineers place far less emphasis on structural analysis tools in electronics. However, as E/E technical advancements produced increasingly smaller components that handle ever increasing amounts of power and heat, the micro-structural integrity of wire bonds, micro-terminals and solder joints in E/E devices have become increasingly important.

Without the tools and skills for CAE modeling, achieving structural integrity, durability and reliability in E/E products, remained dependent on Design-Build-Test-Fix (D-B-T-F) reliability growth processes. These are essentially trial and error experiments with prototype parts that employ a variety of environmental stress and usage durability testing. The time and cost of building and testing prototype E/E modules has been a limiting factor in efforts to accelerate the product development-validation process of automotive E/E equipment in high reliability and harsh environment applications. Furthermore, timing requirements may dictate that prototype modules use surrogate or non- production components which can yield different test results than the final production intent design. POF/RP modeling allows the engineer to simulate and evaluation the production intent part behavior of their design.

CAE APPS

The term “App” refers to “ready to use” application software programs that perform “specific” tasks for the user. Apps differ from general purpose application programs such as spreadsheets, databases or word processor programs that are blank canvases enabling users to create documents, organize data, perform an analysis or create their own applications. Ready to use specific function Apps spares the user from needing to have both functional expertise as well as the programing skills required to create and run their own models.

Engineering Apps are starting to appear to provide a way to resolve the shortage of CAE expertise and reduce the time needed to create custom models and simulations. CAE stress and structural analysis and PoF modeling was originally performed using classical numerical Finite Element Analysis (FEA) for mechanical stress issues and Computational Fluid Dynamics (CFD) for thermal stress issues. These multi-use analysis tools require a significant amount of expertise and time to create and run a custom model for each new product. This burden limited CAE techniques from expanding into new areas, especially electronics where circuit boards hold hundreds to thousands of E/E components that each need to be modeled. A further constraint is that E/E engineers are rarely trained in mechanical structural analysis, material mechanics and stress analysis CAE methods.

The CAE software industry has started to develop CAE Apps and analysis templates as have individual companies that have developed their own, in-house CAE tools. This new generation of CAE solutions provide common, application specific, reusable, semi-automated interface for solving frequently encountered problems and performing regularly needed product optimization tasks that allow non-CAE experts to rapidly perform expert level evaluations [1].

A PoF/RP CAE APP for Electronics

A knowledge based CAE App tool suite called Sherlock ADATM (Automated Design Analysis) has been developed to perform a stress analysis based durability simulation on a virtual model of an E/E module. It then calculates the durability life and reliability of various failure mechanisms for the electronic component and structural elements on the circuit board(s) of the module. This is similar to the way structural durability analysis is performed for vehicle, aircraft and other structural or mechanical systems.

The Sherlock program, from DfR Solutions, is the result of over 20 years of PoF research to identify how and why E/E components and materials fail. Math models of these failure mechanisms have been developed, calibrated, validated and incorporated into the Sherlock program. The App was designed to enable non-CAE experts, to quickly create and perform PoF/RP analysis. This is achieved by a high degree of automation and preloaded libraries of: component models, material properties, design templates, analysis wizards and environmental profiles for specific applications. The automation enables E/E engineers, Printed Circuit Board (PCB) designers and quality/reliability personnel to incorporate virtual reliability growth into the design process.

There are 5 steps in preforming a durability simulation and reliability assessment in the Sherlock CAE App.

1. Project Creation & Design Capture.
2. Life Cycle Characterization.
3. Load Transformation.
4. PoF Durability Simulation, Reliability/Risk Assess.
5. Review Results

Step 1 - Project Creation & Design Capture

This initial step defines the analysis project, its reliability and durability objectives and provides the information needed to create a virtual model of each Print Circuit Board Assembly(s) (PCBAs) in an E/E module. The CAE model is automatically created from standard PCBA Computer Aided Design (CAD) files. These are the same files sent to PCB fabricators and assemblers for use in Computer Aided Manufacturing (CAM) processes. The older Gerber file format, the newer OBD++ CAD-to-CAM format or the IPC-2581 PCB Data Exchange standard can be used to create the virtual PCBA model.

One of the most useful items produced during model creation is the PCB stack up analysis which identifies the size and materials of each of the copper conducting and insulating layer in a multilayer PCB. The Sherlock program has a library of 48 Categories of Material Properties and Characteristics of over 400 PCB Laminates Materials from 20 Global material producers. The board layer geometry info is combined with the material property library to calculate the overall thermal and mechanical performance of the circuit board. The stack up analysis is important because a PCB is the foundation that supports and connects all the components in an electronic device. Knowing the material properties and performance of an actual PCB is needed to determine how the circuit board will react to environmental conditions and how it will transmit stress to its individual electronic component.

The program also has a library of dimensions and material properties of standard E/E components that uses the PCBA's Bill of Material (BOM) E/E part list to create and position virtual component models individual EE components that populate the PCBA. Once the ECAD files are imported, the program automatically self generates the FEA models needed for structural analysis as shown in Figure 1.

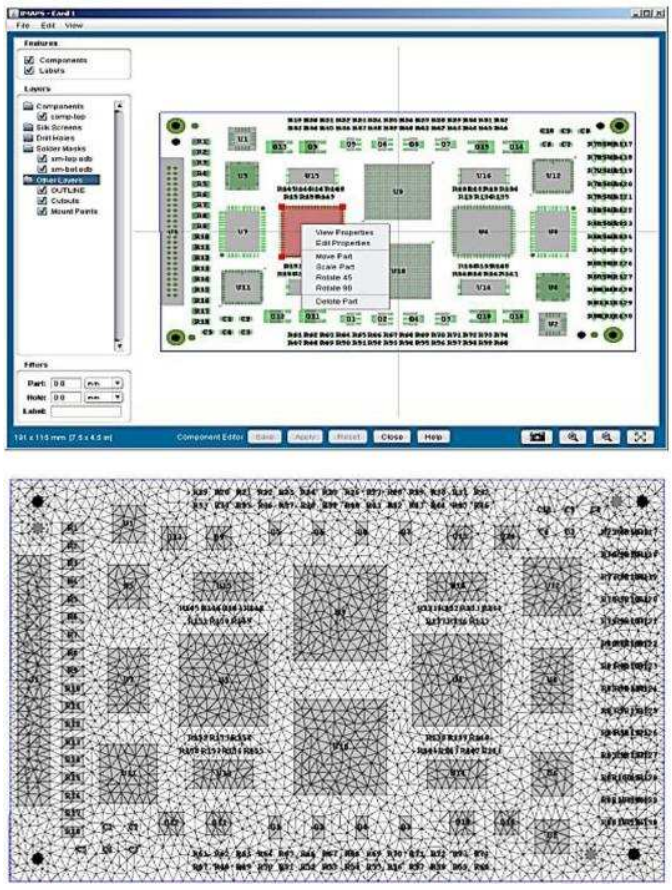

Figure 1. Standard PCBA CAD/CAM data exchange files are uses to automatically create a virtual model of a circuit board assembly (upper) and finite element mesh (lower).

2. Life Cycle Characterization

A PoF/RP durability simulation and reliability assessment evaluates the ability of a specific design to endure the intended environmental and usage stress loading conditions the product is expected to operate in, over its required service life (known as the life profile). The Sherlock CAE App can model a series of: Thermal Cycling Conditions, Harmonic and Random Vibration and Shock events expected over the service life of the electronic module *(See* Figure 2*).*

The life profile is more than simply the environmental range the device is to operate in. It must include the intensity, duration and frequency of the environmental loads and stresses the electronic device is expected to endure over its service life or during a durability or reliability demonstration validation test. Power dissipation self-heating conditions for the overall device or individual component can also be defined when appropriate. The Sherlock CAE App comes with a library of military, automotive and aviation environmental load profiles. Users can also define and save their own profiles for future use.

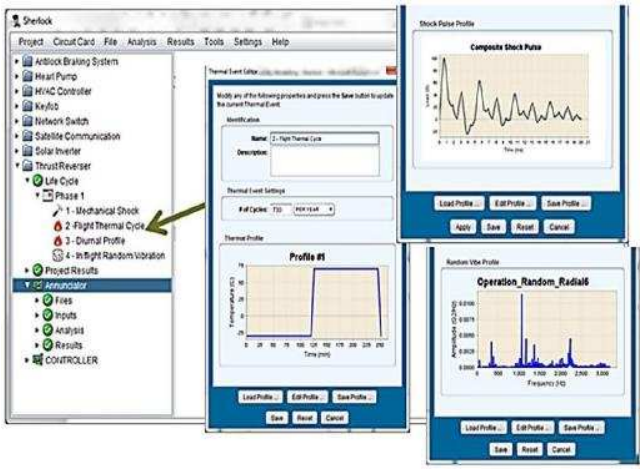

Figure 2. Examples of how environmental condition stress profiles are programmed into the Sherlock PoF CAE Apps.

3. Load Transformation

Once the virtual PCBA model is completed and the stress conditions are defined, the Finite Element Analysis dynamic stress analysis is performed. The FEA simulation determines the stresses and strain conditions related to the environmental and usage loading conditions that are created within or transmitted across the circuit board and applied to all of the circuit board's components *(See* Figure 3*).*

Once the dynamic stress and strain conditions throughout the circuit board and each electronic component on the PCB are known, the Physics of Failure Durability simulation can be performed.

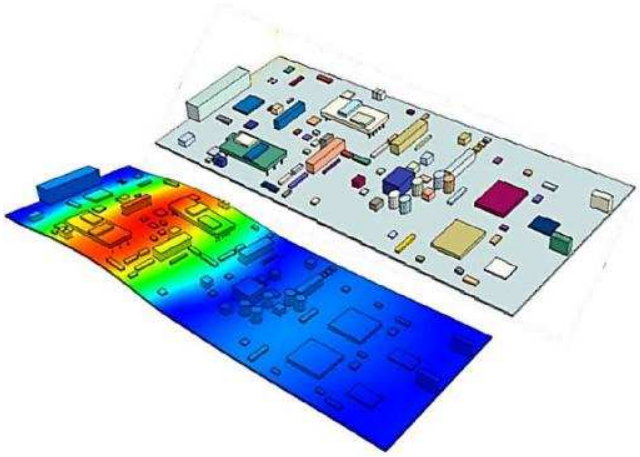

Figure 3. FEM Stress, Strain and Modal Results of an Electronic Circuit Board under Vibration Conditions

4. PoF Durability Simulation, Reliability & Risk Assessments

The FEA stress analysis results automatically become inputs to the various PoF failure mechanism model applicable to the specific PCBA design and its components. The Sherlock CAE App first calculates the mean life for each failure mechanism related to each part type on the PCBA. Then a library of the typical Weibull slope for that failure mechanism acting on each part type (also developed by PoF Research) is referenced to determine the life distribution about the mean. The Sherlock CAE App performs the following wear out and over stress failure simulations and risk assessments, examples of which are shown in Figure 4.

- Thermal Cycling Fatigue of Solder Joints. ◦ Traditional Tin/Lead Solder.
  ◦ SnAgCu based Lead Free Solders.
- Thermal Cycling Fatigue of Circuit Board Vias.
- Random and Harmonic Mechanical Vibration Fatigue of Solder Joints.
  ◦ Traditional Tin/Lead Solder.
  ◦ SAC Lead Free Solder.
- Mechanical Shock Fracture of Solder Joints ◦ Traditional Tin/Lead Solder.
  ◦ SAC Lead Free Solder.
- Repetitive Shock Fatigue of Solder Joints.
  ◦ Traditional Tin/Lead Solder.
  ◦ SAC Lead Free Solder.
- Conductive Anodic Filament Formation Design Rule Check/ Risk Assessment.

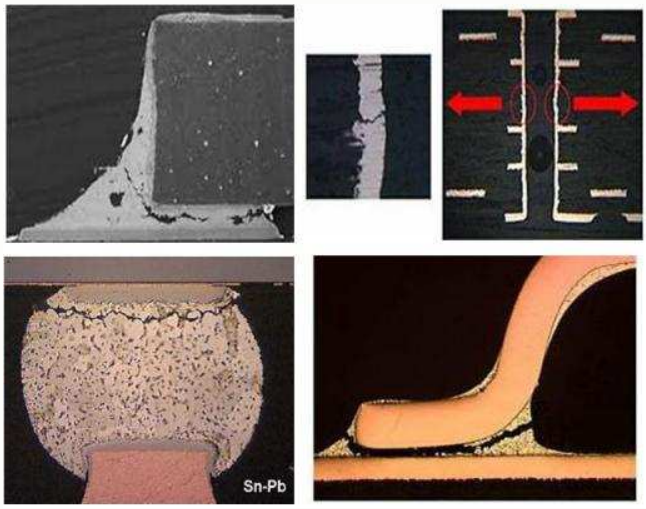

Figure 4. Electronic Structural Field Failure Examples:
- Surface Mount Resistor Solder Fatigue (Upper Left) - Copper Via Barrel Fatigue (Upper Right)
- Ball Grid Array IC Solder Ball Fatigue (Lower Left) - Gull Wing IC Solder Failure (Lower Right).

5. Review Results

Figure 5 shows a plot of the individual and combined accumulated wear out failure risk timeline curves. These curves are calculated from the durability simulations and (in this example) are plotted against a reliability-durability objective of no more than 10% failures (90% Reliability) 10 years in service. The plot uses a reliability metric known as the "Bx" or "Lx" format. This metric defines the "Life Point" (in hours, days or years or cycles) when no more than x% of the units in a population will have failed. The plots reveal when each wear out failure mechanism is calculated to start and its rate of growth over time.

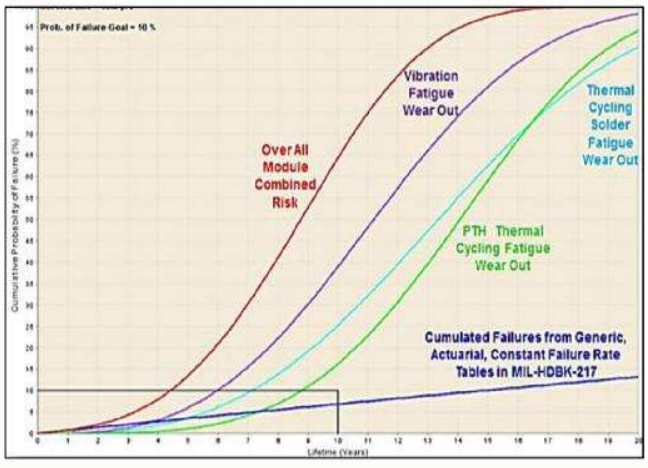

Figure 5. PoF CAE App Durability Simulation Failure Risk Over Life Time Results for an Electronic Module, Plotted Against a 10 year L10 Reliability-Durability Objective.

The Sherlock PoF CAE App also produces a color coded Pareto list that identifies the components or features projected to have the greatest risk of failure for each failure mechanism. The "Bx/Lx" reliability metric is again used by the CAE App program to assign critically-risk color coding where:

- Red = High Failure Risk Within the Expected Life
- Yellow = Moderate Failure Risk
- Green = No Failure Risk Within the Expected Life

This critically-risk color codes are applied to the Pareto list and the component sites in either 2D or 3D virtual models of the PCBA. The color coding enables easy identification and prioritization of the high risk/weak link items, most likely to fail within the life goal defined by the "Bx/Lx" Metric *(See* Figure 6*).* The program also has a user configurable report generator. The user can select desired model information to be combined with various results plots and tables into a modeling results report that is saved in a PDF file format.

Correlation of failure risks to specific failure mechanisms also identifies why items are expected to fail so that effective corrective actions can be implemented to design out the high risk items while the design is still on the CAD screen. This results in a virtual form of Reliability Growth that can be achieved without the time and expense of building prototype modules and running physical reliability growth durability tests. The PoF analysis provides knowledge that enables designers to make enlightened design and manufacturing choices that minimize failure opportunities in order to produce reliability optimized products and systems.

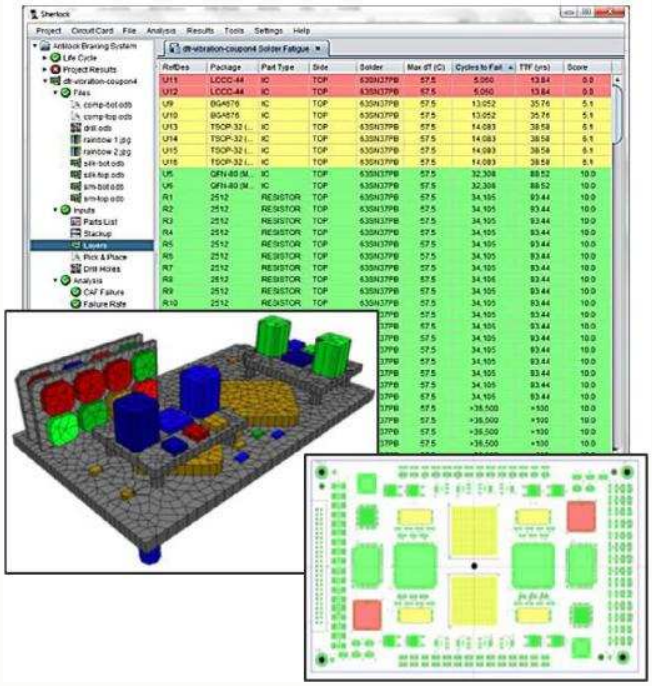

Figure 6. Pareto Risk List 2D & 3D Graphic Representation, Color Coded Component Failure Risk are Outputs Generated for each Failure Mechanism Modeled.

CASE STUDY: SIMULATION AIDED TESTING

An automotive control module containing 750 surface mount E/E components (that included chip capacitors and resistors, electrolytic capacitors, inductors and integrated circuits in SOIC, QFPs, QFNs, PQFNs, BGAs packages) was being developed by Magna Electronics to an OEM customer's specifications. The module's specification required a reliability of at least 99.5% (i.e. ≤ 0.5% failure risk) over an 11 year vehicle life. The module's reliability demonstration/growth test requirements consisted of a rounds of Mixed Environment Reliability Tests (MERT) intended to represent 11 years of severe vehicle usage, included a combination of −40 to 120˚C rapid transition thermal shocks in an unpowered state and Powered Temperature Cycling (TPC) performed while the device was operating.

The power cycle required all module outputs to be activated simultaneous and frequently cycled at 80% of maximum current load conditions. This resulted in a Hex (6 output) Quad Power Driver IC in a QFN-32 package experiencing power dissipation self-heating temperatures of 17˚C above the ambient conditions related to the vibration and thermal cycling conditions required by the device's MERT test profile. The design and prototype builds were already completed prior to the acquiring the Sherlock program.

- The module passed the first round of the MERT reliability growth testing using a prototype PCB in the device.
- When a second round of MERT testing was performed on a production intent version of the PCB failures occurred late in the thermal cycling portion of the test due to fatigue cracks in the solder joints of a QFN-32 Integrated Circuit (IC). Solder thermal cycling expansion/ contraction fatigue is a result of the Coefficient of Thermal Expansion (CTE) mismatch between a circuit board and it components.

A QFN (Quad Flat No-lead) IC is a low profile, Leadless Near Chip Scale Package (LNCSP), IC (see Figure 7) developed for ultra-light, thin, cell phones tablets and other hand-held, telecom electronics, which is the biggest growth market for electronics. IC manufacturers are responding by shifting production of existing and new ICs to these package styles to meet the demands of their high volume, telecom customers.

Without terminal leads that can flex to absorb stress from automotive thermal cycling, vibration and shock conditions, QFN ICs have less solder attachment fatigue durability than an equivalent IC available in leaded packages [7]. As fewer ICs are available in the more robust leaded packages, electronics suppliers are challenged to meet automotive reliability-durability objectives using these newer IC style.

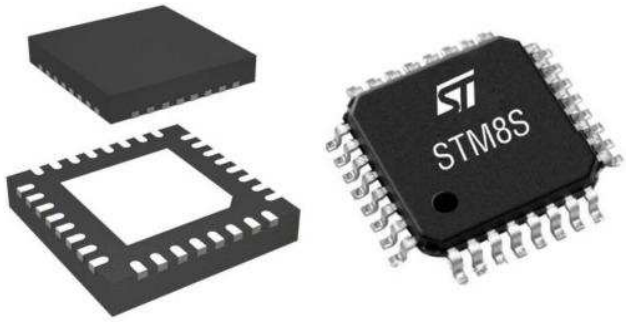

Figure 7. A rigid lead-less QFN-32 IC package (left) compared to a QFP-32 IC (right) which has flexible leads.

Although there had been no changes in the assembly and soldering processes and E/E components, the early prototype PCBs were fabricated by a quick turn PCB supplier and a different fabricator provided the production intent PCBs. The two suppliers used different PCB laminates and solder mask materials, both of which had been previously qualified on different programs. Although the PCB laminates were almost identical in mechanical properties the initial suspicion was that a subtle difference in mechanical properties of the circuit boards had caused the solder fatigue cracks.

Sherlock Analysis

Using the Sherlock ADA CAE App, the two different laminate materials were modeled in a durability simulation to determine if the slight difference in the PCB material would explain the difference in test results. The first modeling results indicated that assuming all other items were equal, the production intent PCB laminate should provide better durability than the prototype PCB material.

Therefore, other parameters that influence solder fatigue were investigated. Cross sections of the QFN-32 IC that passed the initial prototype MERT testing were found to have a solder column thickness >50 microns. Cross sections of the parts that failed in the second round of testing were found to have solder thicknesses as low as 28 microns.

The same amount of solder paste was used on both prototype builds but more solder flowed out from under the IC in the final PC (Product Validation) build, resulting is a thinner weaker solder joint (See Figure 8).

Additional Sherlock Durability simulations were then run to evaluate and quantify the effect of the solder thickness variable factor. A Sherlock durability simulation evaluating the QFN having a 35 micron solder thickness, found that premature solder fatigue failures would occur resulting in the 0.5% accumulated failure limit being exceeded at a durability test point that correlated to 8.7 years in service. This correlated well with the actual test results (See Figure 9).

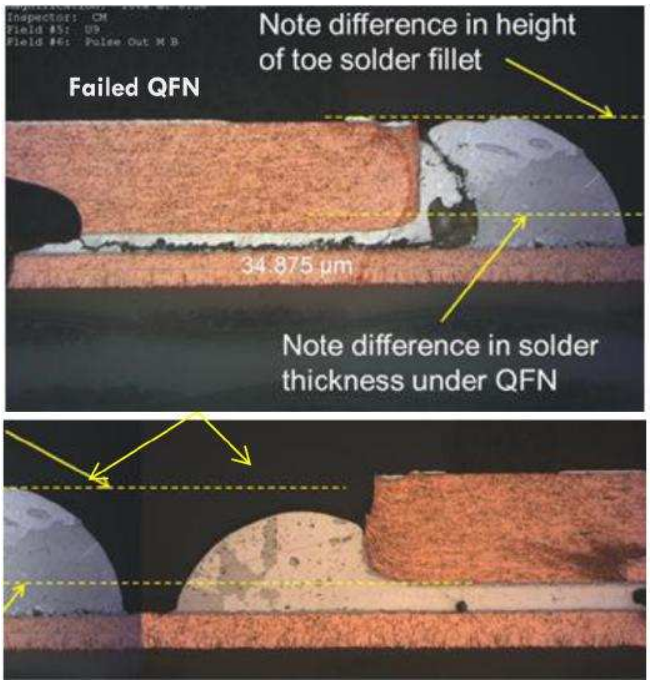

Figure 8. Cross section comparisons found thinner solder thicknesses under the PV Fail d QFN (top) and thicker solder under the QFNs that passed DV testing (bottom).

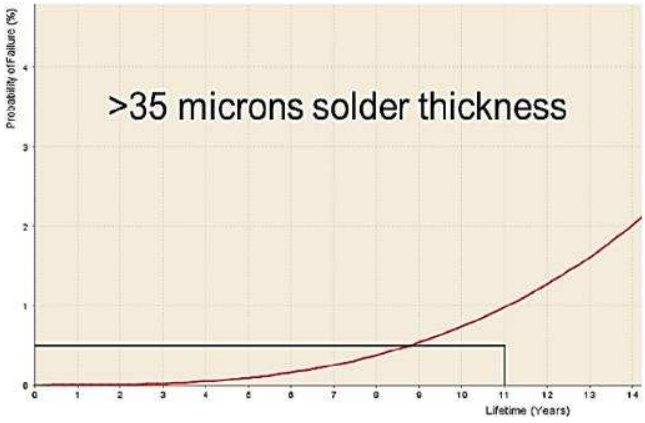

Figure 9. Sherlock durability simulation results found that the 11 year 0.5% solder fatigue objective would be reached in only 8.7 years in service for the QFN with 35um thick solder.

Another durability simulation was run using an assumption of less power dissipation self-heating of the QFN-32 IC leading to a 5˚C reduction of the peak temperature of the part during the thermal cycling portion of the MERT durability life test. The simulation indicated that with this slight reduction in peak thermal stress, the QFN-32 with thinner solder joints would then be able to meet the objective of <0.5% failures by 11 years (See Figure 10).

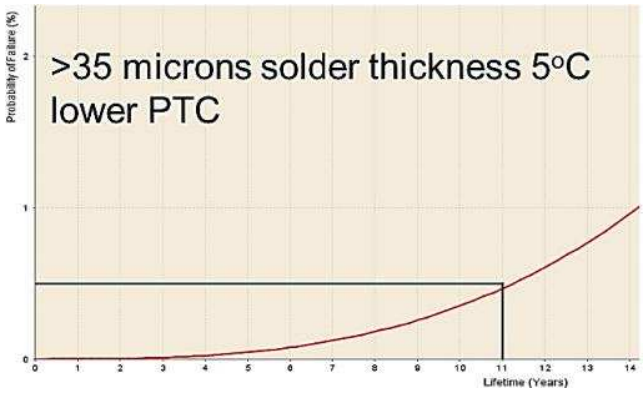

Figure 10. Revised durability simulation indicated that with a slight 5˚C reduction in peak thermal stress, the 11 year 0.5% solder fatigue objective could be met, even with the thinner solder joints.

A third durability simulation was then performed increasing the solder thickness under the QFN to 50 microns. This resulted in a thicker, stronger solder joint that increased the 0.5% fatigue life projects to beyond 15 years (See Figure 11).

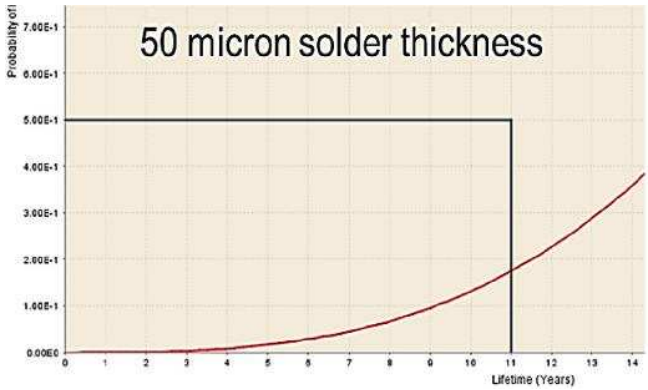

Figure 11. The durability simulation of a 50um solder thickness indicates the 0.5% fatigue life point would be extended to over 15 years to exceed the 11 year objective.

SUMMARY/CONCLUSIONS

With a few days and several rounds of Sherlock PoF durability simulations of the module's circuit board assembly the Sherlock ADA CAE App was found to accurately reproduce test results and then provided insight that correctly identified and quantified the reasons for differences in the MERT durability-reliability growth testing. This resulted in a permanent corrective action to adjust and monitor the circuit board assembly soldering process to ensure that an adequate solder height is always maintained on the sensitive QFN-32 IC.

Obtaining the same results would have otherwise required months of costly sample preparation and physical testing. As a result of this event the Sherlock ADA CAE App has been validated and is being increasing used at Magna Electronics to provide early evaluation of the durability and reliability capabilities and sensitivities of new automotive electronic modules while the design is still on the CAE screen. This

allows reliability concerns to be identified and resolved without the time and expense of tradition physical DBTF reliability growth testing.

The Sherlock ADA tool suite of CAE Apps integrates leading edge Physics of Failure Reliability Science with the latest advancements in semi-automated Computer Aided Engineering Analysis tools. This CAE App allows electrical engineers, PCB designers or QRD personnel to be able to easily and quickly perform the type of structural analysis and durability simulation on their products that have been standard practice used by mechanical engineers on vehicle body, chassis and engine component for decades.

This paper demonstrates the commitment Magna Electronic has for adopting the latest advancement in CAE based product development tools that are enabling the creations of highly reliable, robust automotive electronic products faster, at lower costs, on the first attempt for our customers.

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